AC/DC Drivers

PWM Converter ICs With Built-In 650V MOSFET

BM2PXX4 Series

● Overview

The PWM converter IC for AC/DC "BM2PXX4" provides an optimum system for all products that include an electrical outlet. Support for both isolated and non-isolated configurations makes it possible to easily design a variety of low-power electrical converters.

A 650V startup circuit is built in for lower power consumption. External switching current detection resistors provide greater design flexibility. Current mode control limits the current in each cycle, providing superior bandwidth and transient response performance. Switching frequency is fixed at 65kHz. The frequency is reduced during light loads for greater efficiency. A frequency hopping function is built in, resulting in lower EMI. A 650V MOSFET is also included, simplifying design.

●Basic Specifications

■Operating Supply Voltage Range: VCC 8.9V to 26.0 V
DRAIN: ~ 650 V

■Operating Current: Normal:
(BM2P014): 0.950 mA (Typ.)
(BM2P034): 0.775 mA (Typ.)
(BM2P054): 0.600 mA (Typ.)
(BM2P094): 0.500 mA (Typ.)
Burst Mode: 0.400 mA (Typ.)

■Oscillation Frequency: 65 kHz (Typ.)

■Operating Temperature Range: - 40 deg. to +105 deg.

■MOSFET ON Resistance: BM2P014: 1.4 Ω (Typ.)
BM2P034: 2.4 Ω (Typ.)
BM2P054: 4.0 Ω (Typ.)
BM2P094: 8.5 Ω (Typ.)

● Application Circuit

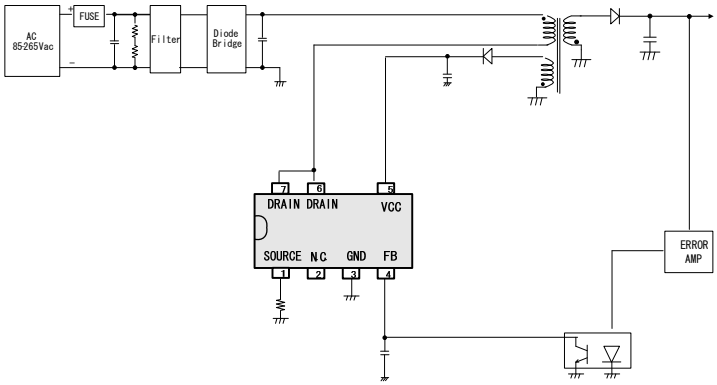


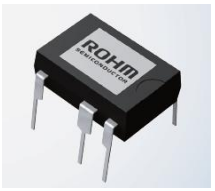
Figure 1. Application Circuit

●Features

■PWM frequency: 65 kHz
■PWM current mode control
■Built-in frequency hopping function
■Burst operation during light loads / Frequency reduction function
■Integrated 650V startup circuit
■Built-in 650 V switching MOSFET
■VCC pin undervoltage protection
■VCC pin overvoltage protection
■SOURCE pin open protection
■SOURCE pin short circuit protection
■SOURCE pin Leading Edge Blanking function
■Per-cycle overcurrent limiter function
■Overcurrent limiter with AC compensation function
■Soft start function
■Secondary overcurrent protection circuit

●Package

DIP7 (9.20 mm × 6.35 mm × 4.30 mm pitch 2.54 mm typ.)



●Applications

AC adapters, TVs, and home appliances (i.e. vacuum cleaners, humidifiers, air cleaners, air conditioners, IH cooking heaters, rice cookers)

●Lineup

Part No.	MOSFET ON Resistance
BM2P014	1.4 Ω
BM2P034	2.4 Ω
BM2P054	4.0 Ω
BM2P094	8.5 Ω

● **Absolute Maximum Ratings (Ta = 25°C)**

Parameter	Symbol	Rating	Unit	Conditions
Maximum voltage 1	Vmax1	-0.3 to 30	V	VCC
Maximum voltage 2	Vmax2	-0.3 to 6.5	V	SOURCE, FB
Maximum voltage 3	Vmax3	650	V	DRAIN
Drain current pulse	I_{DP}	10.40	A	P_W = 10 us, Duty cycle = 1% (BM2P014)
Drain current pulse	I_{DP}	5.20	A	P_W = 10 us, Duty cycle = 1% (BM2P034)
Drain current pulse	I_{DP}	2.60	A	P_W = 10 us, Duty cycle = 1% (BM2P054)
Drain current pulse	I_{DP}	1.30	A	P_W = 10 us, Duty cycle = 1% (BM2P094)
Power dissipation	Pd	1000	mW	
Operating temperature range	Topr	-40 to +105	°C	
Maximum junction temperature	Tjmax	150	°C	
Storage temperature range	Tstr	-55 to +150	°C	

Note1: When mounted on 74.2 × 74.2 × 1.6mm glass epoxy single-layer substrate. Reduce by 8.0 mW/ °C when used above Ta = 25 °C.

● **Recommended Operating Conditions (Ta = 25°C)**

Parameter	Symbol	Rating	Unit	Conditions
Supply voltage range 1	VCC	8.9 to 26.0	V	VCC pin voltage
Supply voltage range 2	V_{DRAIN}	～650	V	DRAIN pin voltage

● **MOSFET Block Electrical Characteristics (Unless otherwise noted, Ta = 25°C)**

Parameter	Symbol	Rating			Unit	Conditions
		Min.	Typ.	Max.		
[MOSFET Block]						
Drain-source voltage	$V_{(BR)DDS}$	650	-	-	V	I_D = 1 mA / V_{GS} = 0 V
Drain leak current	I_{DSS}	-	-	100	uA	V_{DS} = 650V / V_{GS} = 0 V
ON resistance	$R_{DS(ON)}$	-	1.4	2.0	Ω	I_D = 0.25 A / V_{GS} = 10 V (BM2P014)
ON resistance	$R_{DS(ON)}$	-	2.4	3.6	Ω	I_D = 0.25 A / V_{GS} = 10 V (BM2P034)
ON resistance	$R_{DS(ON)}$	-	4.0	5.5	Ω	I_D = 0.25 A / V_{GS} = 10 V (BM2P054)
ON resistance	$R_{DS(ON)}$	-	8.5	12.0	Ω	I_D = 0.25 A / V_{GS} = 10 V (BM2P094)

● **Control IC Block Electrical Characteristics (Unless otherwise noted, Ta = 25°C, VCC = 15 V)**

Parameter	Symbol	Rating			Unit	Conditions
		Min.	Typ.	Max.		
[Circuit current]						
Circuit current (ON) 1	I_{ON1}	700	950	1200	μA	FB = 2.0 (during pulse operation) BM2P014
Circuit current (ON) 1	I_{ON1}	550	775	1050	μA	FB = 2.0 (during pulse operation) BM2P034
Circuit current (ON) 1	I_{ON1}	410	600	790	μA	FB = 2.0 (during pulse operation) BM2P054
Circuit current (ON) 1	I_{ON1}	350	500	650	μA	FB = 2.0 (during pulse operation) BM2P094
Circuit current (ON) 2	I_{ON2}	-	400	500	μA	FB = 0.0 V (during burst operation)
[VCC pin protection function]						
VCC UVLO voltage 1	V_{UVLO1}	12.50	13.50	14.50	V	When VCC rises
VCC UVLO voltage 2	V_{UVLO2}	7.50	8.20	8.90	V	When VCC drops
VCC UVLO hysteresis	V_{UVLO3}	-	5.30	-	V	$V_{UVLO3} = V_{UVLO1} - V_{UVLO2}$
VCC OVP voltage 1	V_{OVP1}	26.0	27.5	29.0	V	When VCC rises
VCC OVP voltage 2	V_{OVP2}		23.5		V	When VCC drops
Latch release VCC voltage	V_{LATCH}	-	V_{UVLO2}-0.5	-	V	
VCC recharge start voltage	V_{CHG1}	7.70	8.70	9.70	V	
VCC recharge stop voltage	V_{CHG2}	12.00	13.00	14.00	V	
Latch mask time	T_{LATCH}	50	100	150	us	
Thermal shutdown temperature	T_{SD}	110	-	-	°C	Control IC block
[PWM mode DC/DC driver block]						
Oscillation frequency 1	F_{SW1}	60	65	70	KHz	FB = 2.00 V
Oscillation frequency 2	F_{SW2}	20	25	30	KHz	FB = 0.40 V
Frequency hopping range 1	F_{DEL1}	-	4.0	-	KHz	FB = 2.0 V
Hopping fluctuation frequency	F_{CH}	75	125	175	Hz	
Soft start time 1	T_{SS1}	0.30	0.50	0.70	ms	
Soft start time 2	T_{SS2}	0.60	1.00	1.40	ms	
Soft start time 3	T_{SS3}	1.20	2.00	2.80	ms	
Soft start time 4	T_{SS4}	4.80	8.00	11.20	ms	
Maximum duty	D_{max}	68.0	75.0	82.0	%	
FB pin pull-up resistance	R_{FB}	23	30	37	kΩ	
FB / SOURCE gain	Gain	-	4.00	-	V/V	
FB burst voltage	V_{BST}	0.300	0.400	0.500	V	When FB drops
Frequency reduction start FB voltage	V_{DLT}	1.100	1.250	1.400	V	
FB OLP voltage 1a	V_{FOLP1A}	2.60	2.80	3.00	V	Overload detection (when FB rises)
FB OLP voltage 1b	V_{FOLP1B}	-	2.60	-	V	Overload detection (when FB drops)
FB OLP ON timer	T_{FOLP1}	40	64	88	ms	
FB OLP start timer	T_{FOLP1b}	26	32	38	ms	
FB OLP OFF timer	T_{FOLP2}	358	512	666	ms	
[Overcurrent detection block]						
Overcurrent detection voltage	V_{CS}	0.380	0.400	0.420	V	Ton = 0 us
Overcurrent detection voltage SS1	V_{CS_SS1}	-	0.100	-	V	0 [ms] ~ Tss1 [ms]
Overcurrent detection voltage SS2	V_{CS_SS2}	-	0.150	-	V	TSS1 [ms] ~ TSS2 [ms]
Overcurrent detection voltage SS3	V_{CS_SS3}	-	0.200	-	V	TSS2 [ms] ~ TSS3 [ms]
Overcurrent detection voltage SS4	V_{CS_SS4}	-	0.300	-	V	TSS3 [ms] ~ TSS4 [ms]
Leading edge blanking time	T_{LEB}	-	250	-	ns	
Overcurrent detection AC compensation factor	K_{CS}	12	20	28	mV/us	
SOURCE pin short protection voltage	V_{CSSHT}	0.020	0.050	0.080	V	
[Start circuit block]						
Start current 1	I_{START1}	0.100	0.500	1.000	mA	VCC = 0 V
Start current 2	I_{START2}	1.000	3.000	6.000	mA	VCC = 10 V
OFF current	I_{START3}	-	10	20	uA	Inflow current from DRAIN pin after UVLO is canceled. (when MOSFET is OFF)
Start current switching voltage	V_{SC}	0.800	1.500	2.100	V	

●Pin Descriptions

Table1. I/O Pin Functions

NO.	Pin Name	I/O	Function	ESD Diode	
				VCC	GND
1	SOURCE	I/O	MOSFET SOURCE pin	○	○
2	N.C.	-	-	-	-
3	GND	I/O	GND pin	○	-
4	FB	I	Feedback signal input pin	-	○
5	VCC	I	Power supply input pin	-	○
6	DRAIN	I/O	MOSFET DRAIN pin	-	-
7	DRAIN	I/O	MOSFET DRAIN pin	-	-

●I/O Equivalent Circuit Diagrams

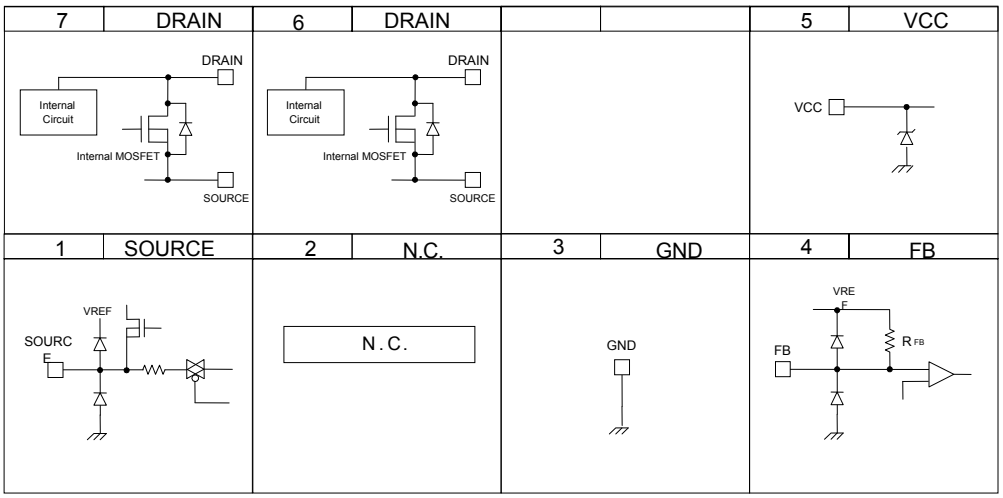


Figure 2. I/O Equivalent Circuit Diagrams

●Block Diagram

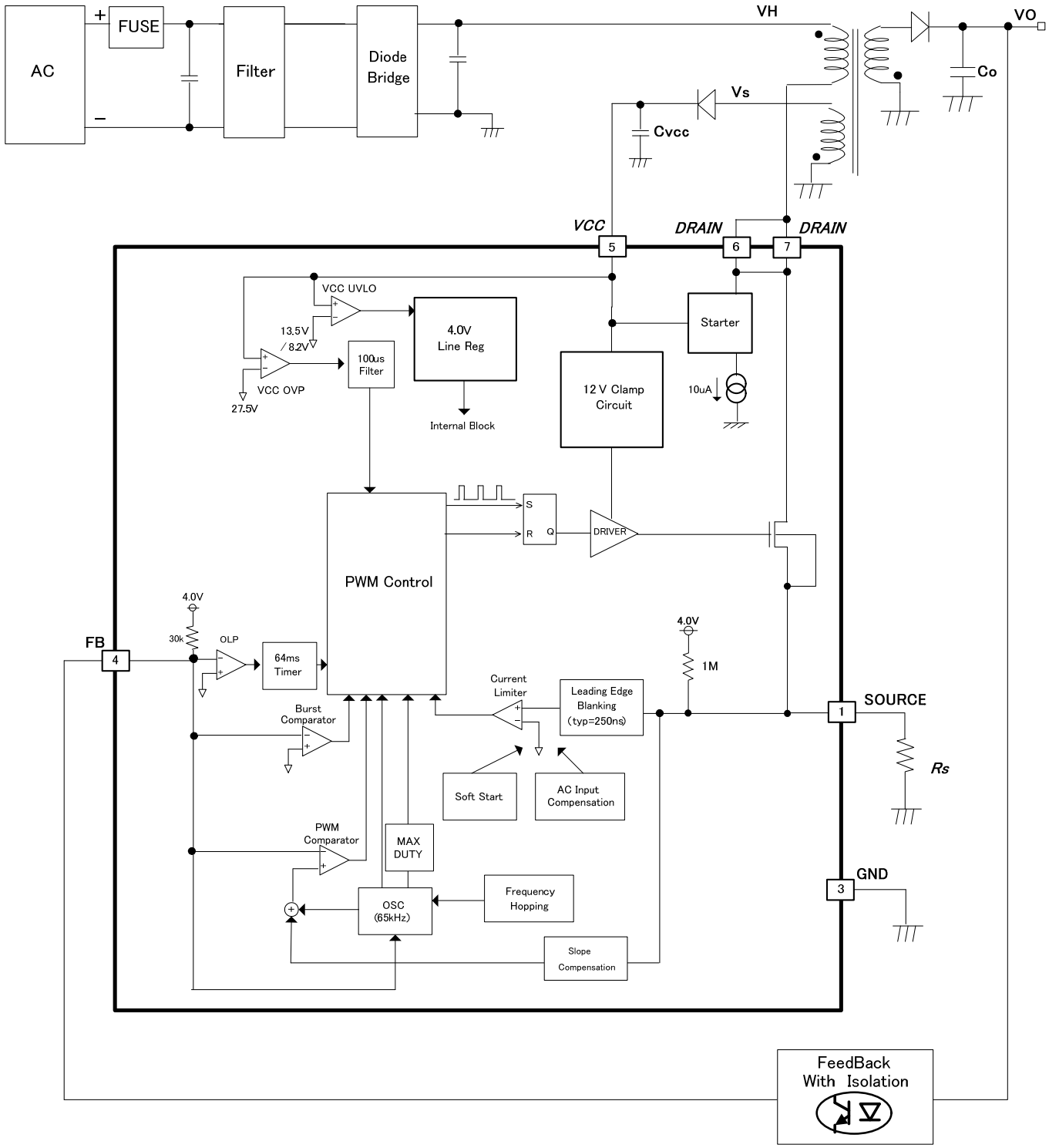


Figure 3. Block Diagram

● Application Description for Each Block

(1) Startup Circuit (DRAIN: Pin 6 and Pin 7)

This IC has a built-in startup circuit (650V withstand voltage). This enables both low standby power and high-speed startup. After startup, the only power consumption is due to the idling current I_{START3} (10uA typ).

Ex.) When Vac=100V, startup circuit power consumption is:
PVH=100V * √2 * 10uA = 1.41mW

Ex.) When Vac=240V, startup circuit power consumption is:
PVH=240V * √2 * 10uA=3.38mW

Startup time reference values are shown in Figure 6. For example, when C_{VCC}=10uF, the VCC pin can be charged in 0.1 seconds or less.
When the VCC pin has been shorted to GND, ISTART1 current flows as in Figure 5.

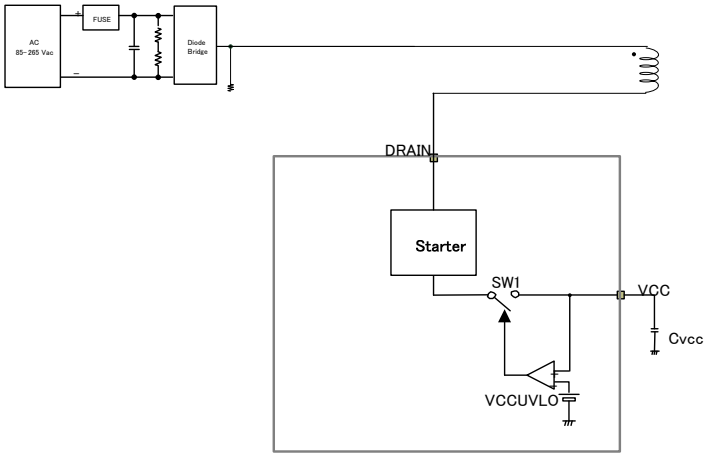


Figure 4. Startup Circuit Block Diagram

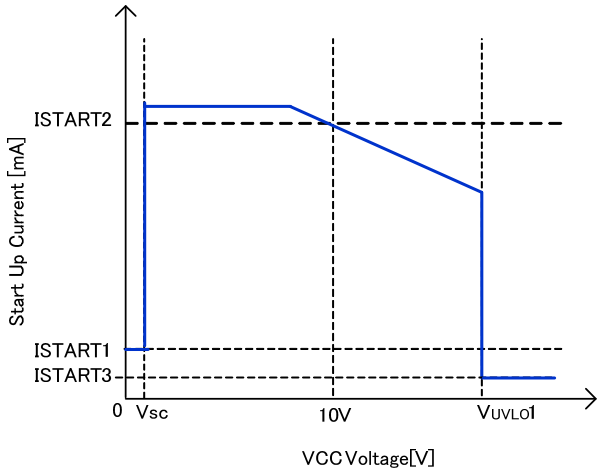


Figure 5. Startup Current vs VCC Voltage

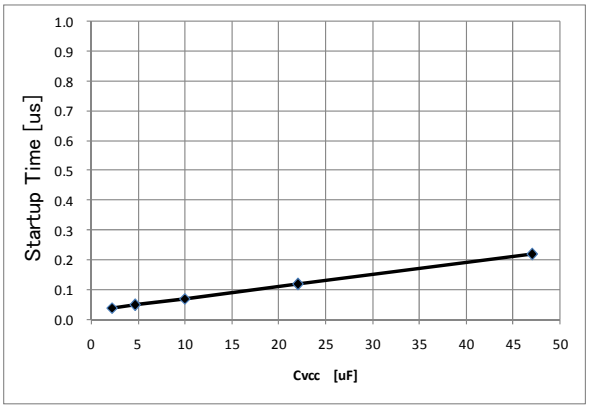


Figure 6. Startup Time (Reference Values)

(*Startup current flows from the DRAIN pin)

Ex.) When Vac=100V, startup circuit power consumption is:
PVH=100 V*√2*10uA=1.41mW

Ex.) When Vac=240V, startup circuit power consumption is:
PVH=240 V*√2*10uA=3.38mW

Application Notes

The operating waveforms at startup are shown in Figure 7.

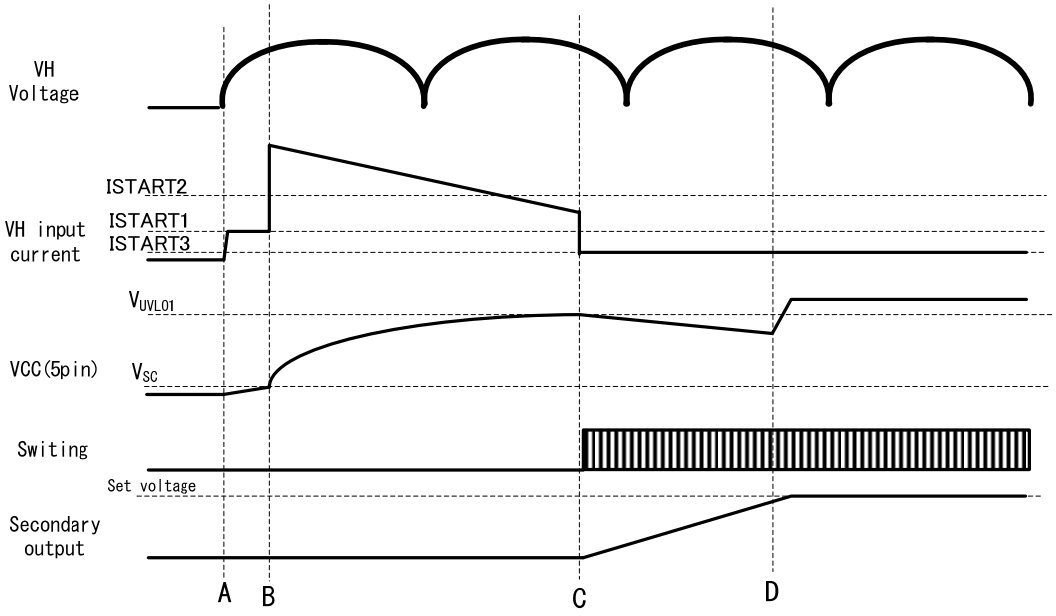


Figure 7. Startup Waveforms

A: VH voltage is applied when plugged into the outlet. At that time, charging starts from the VH pin to the VCC pin via the startup circuit.
Because VCC is less than V_{SC} (0.8V typ.), the VH input current is limited to ISTART1 by the VCC pin short circuit protection function.

B: Since VCC voltage exceeds V_{SC} (0.8V typ.), VCC short circuit protection is cancelled and current flow is from the VH input current.

C: Since VCC voltage exceeds V_{UVLO1} (13.5V typ.), the startup circuit is stopped and VH input current flow is only ISTART3 (10uA typ.).
When switching starts, the secondary output begins to increase, but because the secondary output is low, the VCC pin voltage drops. The VCC drop rate is determined by the IC current consumption, the capacitance of the VCC pin capacitor, and the load current connected to the VCC pin. (V/t = Cvcc/Icc)

D: Since the secondary output has risen to a constant voltage, voltage is applied to the VCC pin from the auxiliary windings, stabilizing VCC voltage.

(2) Startup Sequences (Soft Start Operation, Light Load Operation, Auto Recovery Operation During Overload Protection)

Startup sequences are shown in Figure 8. Please see below for detailed descriptions.

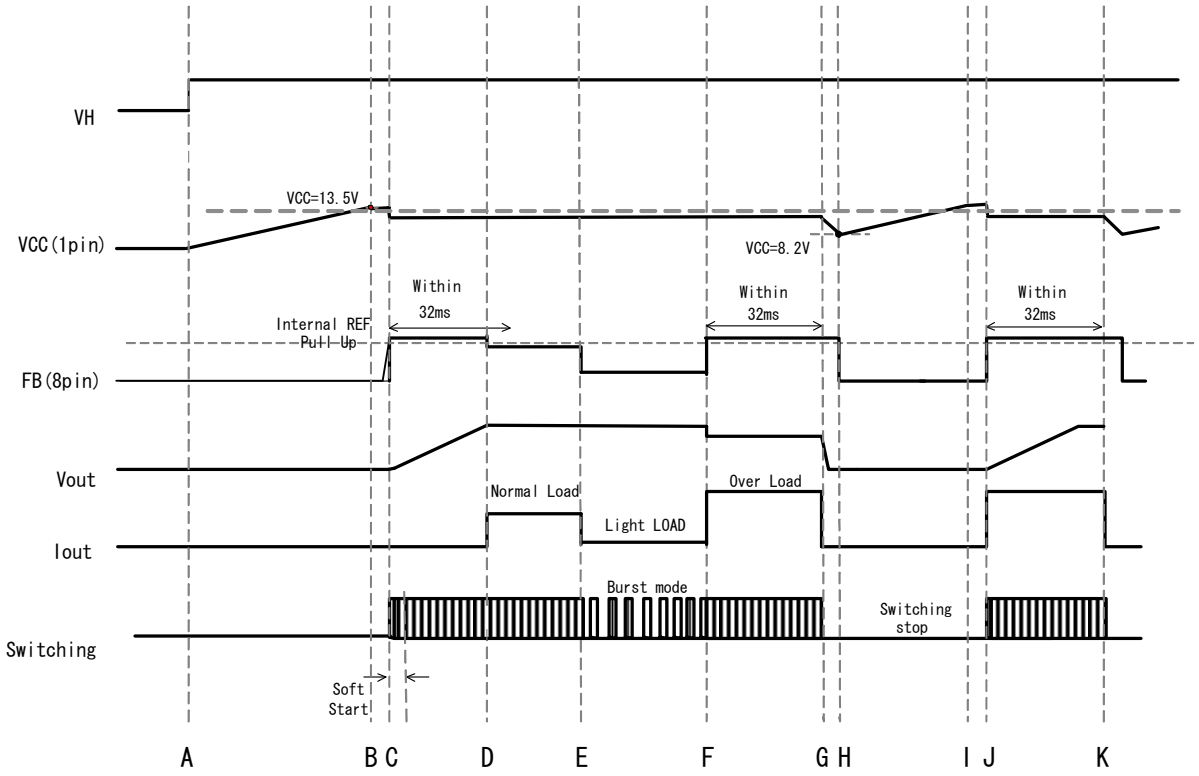


Figure 8. Startup Sequence Time Chart

A : Input voltage VH is applied

B: The VCC voltage rises, and when the VCC voltage exceeds V_{UVLO1} (13.5V typ) this IC begins to operate.
When protection functions (VCC, SOURCE, FB pin, temperature) are determined to be normal, switching operation begins. At this time, the VCC pin voltage drops based on the current consumption. When VCC is less than V_{CHG1} (8.7V typ.), the startup circuit operates to prevent startup errors, and VCC is charged. Once started, charging continues until VCC exceeds V_{CHG1} (13.0V typ.). See item (3-2) above regarding startup circuit operation.
During the period from the start of operation until the secondary output voltage becomes constant, VCC voltage drops based on the VCC pin current consumption, so be sure to set VCC voltage greater than V_{UVLO2} (8.2V typ.) until switching is started.

C: With the soft start function, excessive rises in voltage and current are prevented by changing the overcurrent detection voltage for the SOURCE pin during soft start from V_{CC_SS1} to V_{CC_SS4} and restricting the overcurrent limiter value. See Table 2 below regarding V_{CC_SS}.

Table 2. Overcurrent Detection Voltage at Startup

Soft Start	Vlim1
Start ~ 0.5 ms	0.10 V (12%)
0.5 ms～1 ms	0.15 V (25%)
1 ms～2 ms	0.20 V (50%)
2 ms～8 ms	0.30 V (75%)
8 ms～	0.400 V (100%)

D: When the switching operation starts, the output voltage VOUT rises.
After switching has started, set the output voltage VOUT to within T_{FOLP1b} (32ms typ.) to become the rated voltage.

E: When the FB voltage is less than V_{BST} (0.40V typ.) during light loads, burst operation occurs to suppress power consumption.
During burst operation, operation is in low current consumption mode.

F: When FB voltage exceeds V_{FOLP1A} (2.8V typ.), overload operation occurs.

G: When FB voltage exceeds V_{FOLP1A} (2.8V typ.) continuously for T_{FOLP1} (64ms typ.), switching is stopped for T_{OLPST} (512 ms typ.) by the overload protection circuit.
When FB voltage is less than V_{FOLP1B}, the IC's internal timer T_{FOLP1} (64ms typ.) is reset.

H: Restart occurs when the VCC voltage is less than V_{UVLO2} (7.7V typ.).

I: The IC's circuit current drops and the VCC voltage rises. (Same as B)

J: Same as F

K: Same as G

(3) VCC Pin Protection Function

This IC includes a VCC pin undervoltage protection function (UVLO) and overvoltage protection function (OVP), as well as a VCC charge function that operates when the VCC voltage has dropped.
The VCC UVLO and OVP functions prevent damage to the switching MOSFET that can occur when the VCC voltage drops or becomes excessive.
When the VCC voltage has dropped, the VCC charge function charges from a line with higher voltage than the startup circuit and stabilizes the secondary output voltage.

(3-1) VCC UVLO/OVP Functions

VCC UVLO is an auto-recovery type comparator with voltage hysteresis, while VCC OVP is simply an auto-recovery type comparator. A delay time of T_{LATCH} (100us typ.) is built into VCC OVP. This performs detection when the VCC pin voltage exceeds V_{OVP} (27.5V typ.) continuously for T_{LATCH} (100us typ.).
This function prevents detection errors due to VCC pin surges, etc.

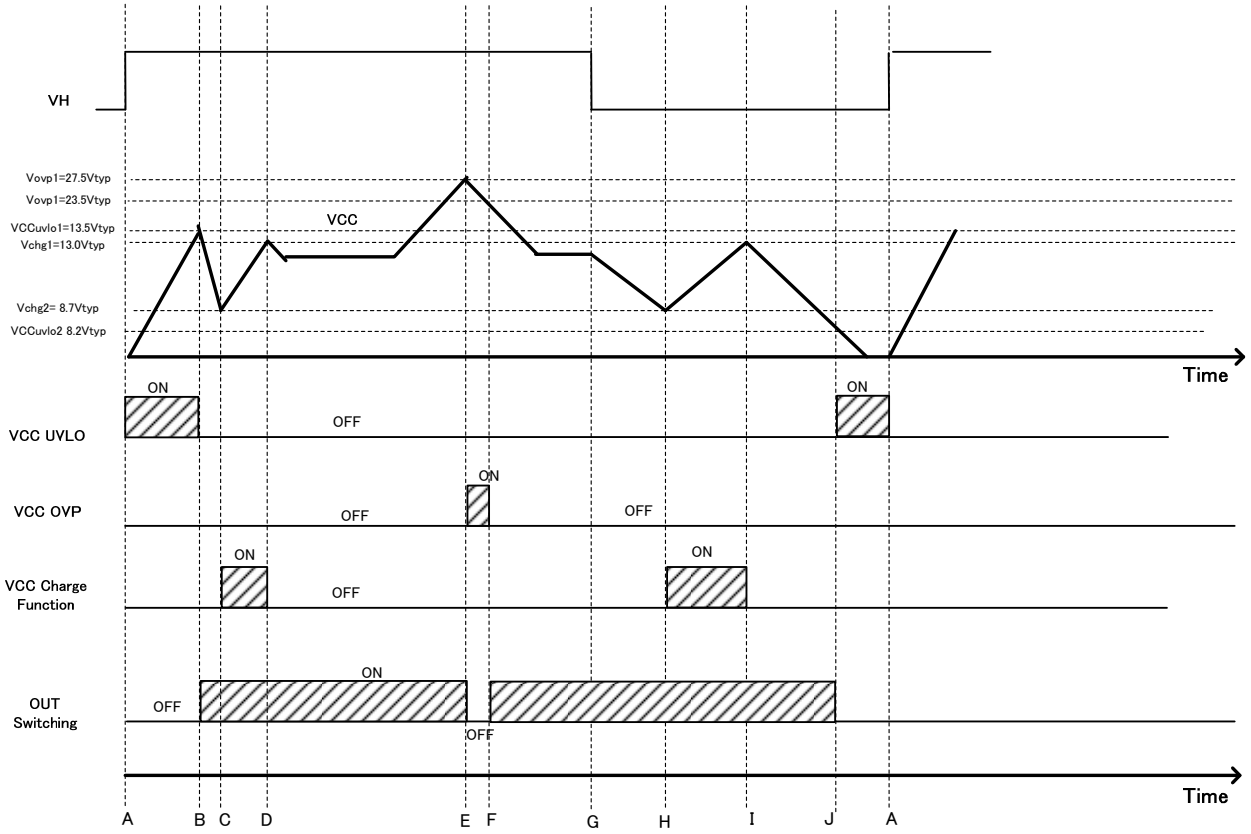


Figure 9. VCC UVLO / OVP Time Chart

A: DRAIN pin voltage is supplied and the VCC pin voltage begins to rise.
B: When the VCC pin voltage exceeds V_{UVLO1}, the VCC UVLO function is canceled and DC/DC operation starts.
C: When the VCC pin voltage is less than V_{CHG1}, the VCC charge function operates and the VCC pin voltage rises.
D: When the VCC pin voltage exceeds V_{CHG2}, the VCC charge function stops.
E: When the VCC pin voltage exceeds V_{OVP1} continuously for T_{LATCH} (100us typ.), switching is stopped by the VCC OVP function.
F: When the VCC pin voltage is less than V_{OVP2}, DC/DC operation is restarted.
G :The high voltage line VH drops.
H: Same as C
I: Same as D.
J: When VCC is less than V_{UVLO2} the VCC UVLO function operates.

・VCC pin capacitance

To ensure stable operation of the IC, set the VCC pin capacitance value to 1 uF or above.

Please note that if the capacitor for the VCC pin is too large, the response of the VCC pin to the secondary output will be delayed. Also, in cases where the transformer has a low degree of coupling, a large surge is generated at the VCC pin, which may damage the IC. In such instances, insert a resistance between 10Ω and 100Ω on the path between the diode and capacitor after the auxiliary winding. As for constants, perform a waveform evaluation of the VCC pin and enter settings that will prevent any surges at the VCC pin from exceeding the absolute maximum rating for the VCC pin.

・VCC OVP voltage protection settings for increased secondary output

The VCC pin voltage is determined by the secondary output and the transformer ratio (Np:Ns). Therefore, when the secondary output becomes large, it can be protected by VCC OVP.
The VCC OVP protection settings are as follows.

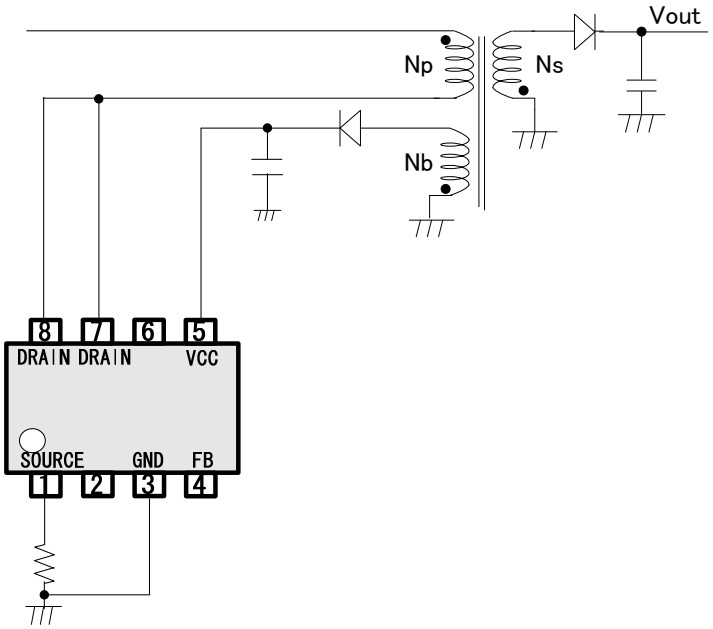


Figure 9. VCC OVP Settings

This is determined by VCC voltage = Vout x Nb/Ns. (Vout: Secondary output, Nb: No. of auxiliary winding turns, Ns: No. of secondary winding turns).

When secondary output increases by 1.3x and protection is desired, set the number of winding turns so that 1.3 x Vout x (Nb/Ns) exceeds V_{OVP1}.
For VCC OVP protection, since there is a T_{LATCH} (100us typ.) blanking time, VCC OVP protection cannot be detected for instantaneous surges at the VCC pin.
However, VCC OVP is detected when the VCC pin voltage becomes higher than V_{OVP1} for at least the T_{LATCH} period (i.e. due to effects from low degree of transformer couplings), so an application evaluation should be done to check this before setting VCC OVP.

(3-2) VCC Charge Function

The VCC charge function operates when the VCC pin voltage exceeds V_{UVLO1} and the IC starts up. Afterward, the VCC pin voltage drops to less than V_{CHG1}. At that time, the VCC pin is charged from the VH pin via the startup circuit. This operation prevents VCC startup errors.
VCC pin is charged, and charging is stopped when VCC pin exceeds V_{CHG2}. This operation is shown in Figure10.

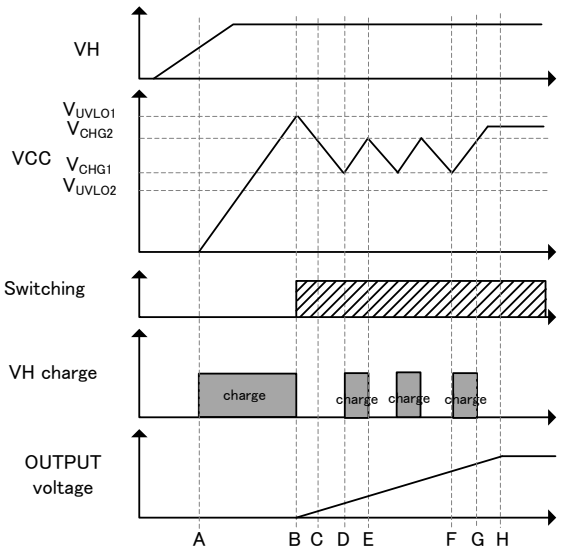


Figure 10. VCC Pin Charge Operation

A: The DRAIN pin voltage rises and the VCC charge function starts charging the VCC pin.
B: When the VCC pin voltage exceeds V_{UVLO1}, the VCC UVLO function is cancelled, the VCC charge function is stopped, and DC/DC operation starts.
C: At startup, the output voltage is low, so the VCC pin voltage drops.
D: When VCC pin voltage is less than V_{CHG1}, the VCC charge function operates and the VCC pin voltage rises.
E: When VCC pin voltage exceeds V_{CHG2}, the VCC charge function is stopped.
F: When VCC pin voltage is less than V_{CHG1}, the VCC charge function operates and the VCC pin voltage rises.
G: When VCC pin voltage exceeds V_{CHG2}, the VCC charge function is stopped.
H: Output voltage startup ends, and the VCC pin is charged by the auxiliary windings to stabilize the VCC pin.

(4) DC/DC Driver (PWM Comparator, Frequency Hopping, Slope Compensation, OSC, Burst)

(4-1) Basic PWM Operations

Figure 11 shows a basic PWM block diagram and Figure 12 illustrates basic PWM operations.

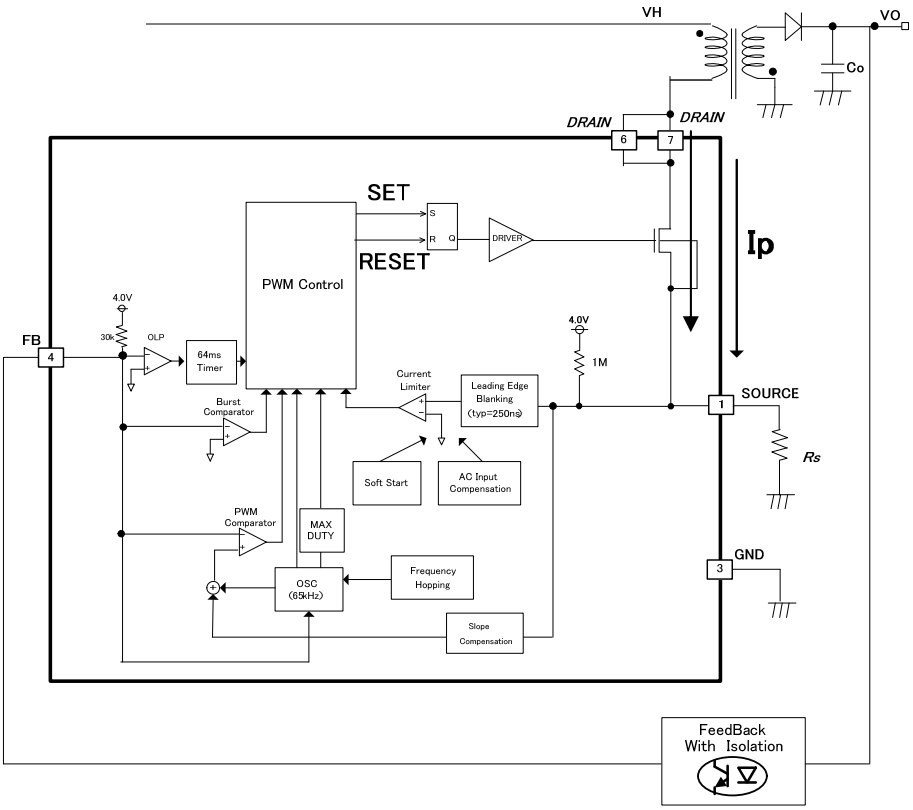


Figure-11. Block Diagram of Internal IC PWM Operations

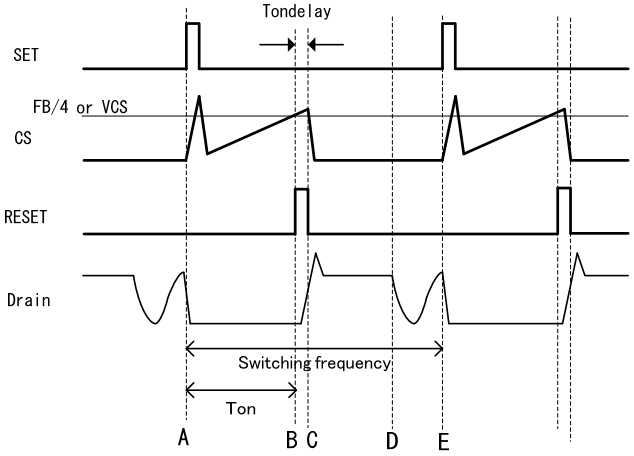


Figure-12. Basic PWM Operations

A: A SET signal is output from the oscillator in the IC, and the MOSFET is turned ON.
At that time, the capacitance between the MOSFET's drain and source becomes discharged, and noise is generated at the SOURCE pin.
This noise is referred to as the Leading Edge.
This IC has a built-in noise filter. [See (6)]
As a result of this filter and delay time, the minimum pulse width of the IC is 800ns (typ).
Afterward, current flows to the MOSFET and the Vcs = Rs * Ip voltage is supplied to the SOURCE pin

B: When SOURCE pin voltage rises to become greater than the FB pin voltage/Gain (4 typ.) or the overcurrent detection voltage Vcs, the RESET signal is output and the MOSFET is turned off.

C: There is a delay time Tondelay between the time of point B and actual turn-off. This time is the result of changes in maximum power that occur based on the AC voltage. This IC includes a function that suppresses these changes. [See (5-4)]

D: The energy that accumulates in the transformer during Ton is discharged to the secondary side, and the drain voltage starts to oscillate freely based on the transformer Lp value and the MOSFET Cds (drain-source capacitance).

E: Since the switching frequency within the IC is predetermined, SET signal output from the internal oscillator occurs for a set period starting from point A, and the MOSFET is turned on.

(4-2) Frequency Operations

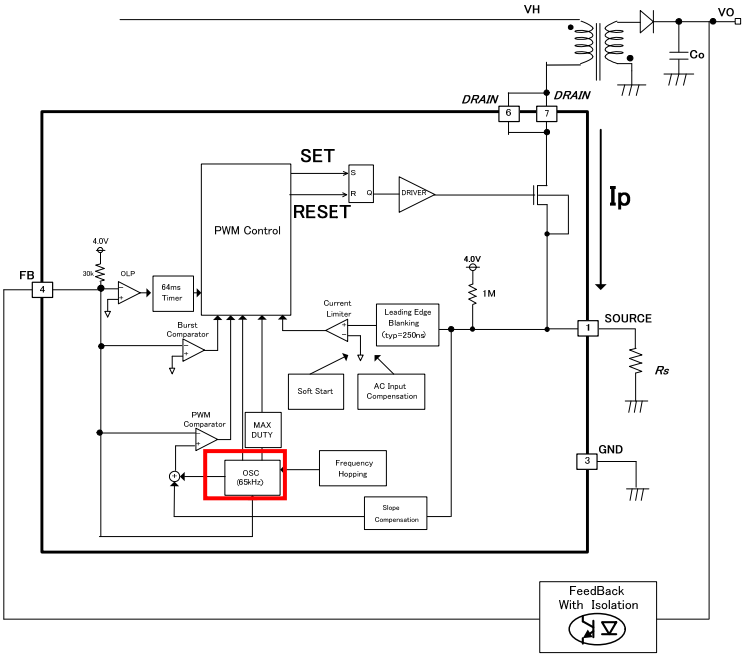


Figure-13. PWM Operations in the IC

The PWM frequency is generated by the OSC block (internal oscillator) in Figure 13.
This oscillator has a switching frequency hopping function and the switching frequency fluctuates as shown in Figure 14.
The fluctuation cycle is 125Hz. Due to this frequency hopping function, the frequency spectrum is dispersed and the frequency spectrum peak is lowered. This increases the margin for EMI testing.

Current mode PWM control is performed.

The switching frequency (65kHz typ.) is fixed by an on-chip oscillator.
A switching frequency hopping function is built in, and the switching frequency fluctuates as shown in Figure 14.
The fluctuation cycle is 125Hz.

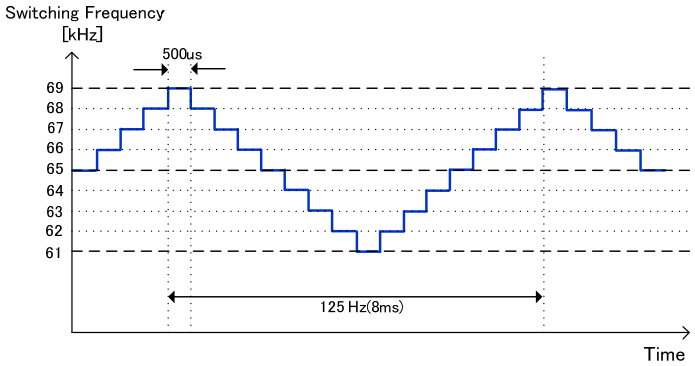


Figure 14. Frequency Hopping Function

MAXDUTY is fixed at 75% (typ) and MIN pulse width is fixed at 800ns (typ).
Under current mode control, if the duty cycle exceeds 50% sub harmonic oscillation may occur. A slope compensation is built in as a countermeasure.

Burst mode and frequency reduction circuits are built in to ensure low power consumption during light loads.
The FB pin is pulled up by R_{FB} (30kΩ typ.) for the internal power supply. The FB pin voltage changes based on the secondary output voltage (secondary load output). The FB pin voltage is monitored before switching to burst mode operation or frequency reduction operation.
The FB voltage and DC/DC operation mode are shown in Figure 15.

・mode1: Burst operation
・mode2: Frequency reduction operation (reduces maximum frequency.)
・mode3: Fixed frequency operation (operates at maximum frequency.)
・mode4: Overload operation (overload status is detected and pulse operation is stopped.)

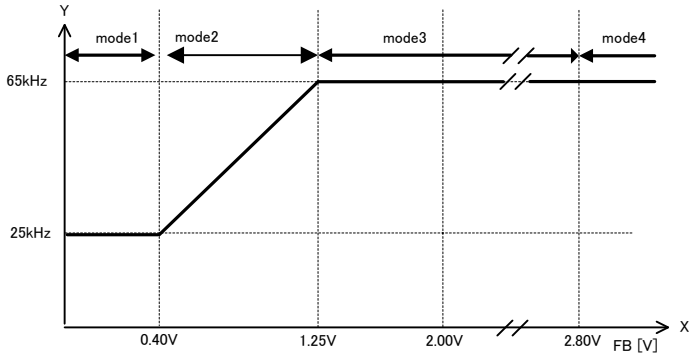


Figure 15. Switching Operation Mode Change Based on FB Pin Voltage

(5-1) Overcurrent Detection Operation

R_{FB} (30 kΩ typ) is used as pull-up resistance for the FB pin with regard to the internal power supply (4.0 V).
When the load of the secondary output voltage (secondary load power) changes, the photocoupler current changes, and therefore the FB pin voltage also changes.
The FB voltage VFB is determined by the equation FB Voltage = 4V - IFB. (IFB: Photocoupler Current)
For example, when the load becomes heavier, the FB current is reduced, and the FB voltage rises.
When the load becomes lighter, the FB current increases, and the FB voltage drops.
In this way, the secondary voltage is monitored by the FB pin.

The FB pin voltage is monitored, and if the load becomes lighter (if FB voltage drops), burst mode operation or frequency reduction operation is executed.
Figure 16 shows the SOURCE detection voltage with regard to the FB voltage.

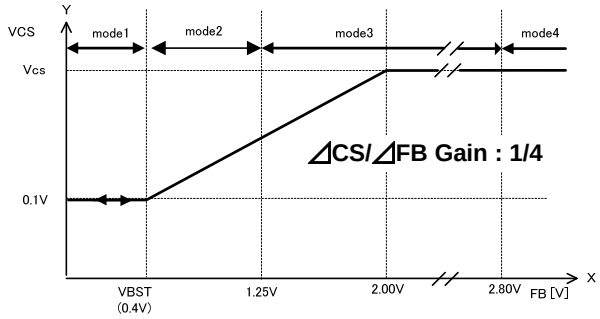


Figure 16. FB Voltage vs SOURCE Voltage Characteristics

When FB voltage is less than 2.0V or when the SOURCE voltage exceeds the FB voltage / Gain (4 typ.), the MOSFET is turned off.
(See time point C in Figure 12.)
When the FB voltage exceeds 2.0 V, the SOURCE voltage = Vcs + Kcs * Ton. Kcs * Ton is for AC voltage compensation. (See 5-2.)
Therefore, peak current Ip is determined as: Ip = Vcs1 / Rs.
The current value for the MOSFET should be set with a margin with regard to the Ip value obtained from this formula.

Maximum power is determined as Pmax = 1/2 x Lp x Ip^2 x Fsw. (Lp: primary inductance value, Ip: primary peak current, Fsw: switching frequency)

Vcs1 is determined as Vcs1 = Vcs (0.4V typ.) + Kcs (typ.= 20) * Ton + Vdelay.
Vdelay is the amount of SOURCE voltage increase during the delay time Tondelay between B and C in Figure 12.
This is calculated as Vdelay = Vin / Lp * Tondelay * Rs.

(5-2) Overcurrent Limiter

This IC integrates an AC voltage compensation function that performs compensation for AC voltage by increasing the overcurrent limiter level over time. In the equation below, (A) and (B) are assigned values similar to those for AC 100V and AC 200V to perform compensation.

$$Vcs1 = Vcs\ (0.4V\ typ.) + \underbrace{Kcs\ (typ.= 20) * Ton}_{(A)} + \underbrace{Vdelay}_{(B)}$$

These operations are shown in Figures 17,18, and 19.

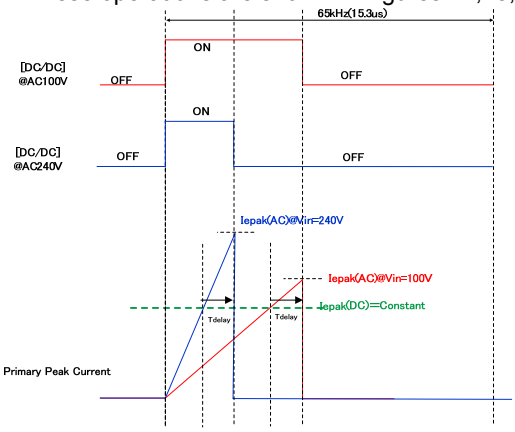


Figure 17. Without AC Voltage Compensation Function

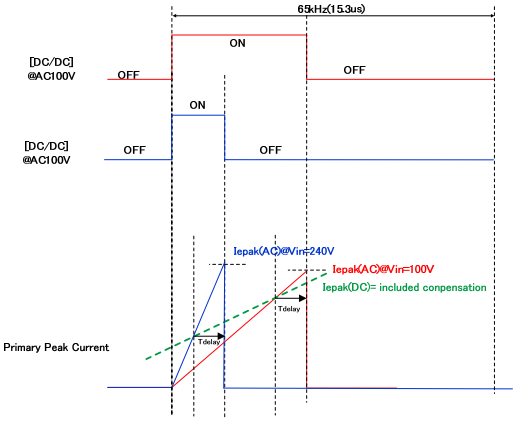


Figure 18. With AC Voltage Compensation Function

The primary peak current during overload mode is defined as follows.

$$\text{Primary peak current } \underline{I_{peak} = V_{cs} / R_s + Kcs * Ton / R_s + V_{in} / L_p * Tondelay}$$

V_{cs}: Overcurrent limiter voltage in IC, R_s: Current detection resistor, V_{in}: Input DC voltage, L_p: Primary peak current, Ton_{delay}: Delay time after overcurrent limiter detection

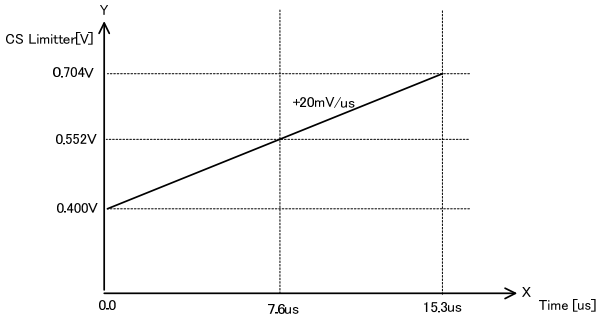


Figure 19. Overcurrent Limiter Voltage

(6) L.E.B. Blanking Time

When the driver MOSFET is turned on, a surge current is generated at time point A in Figure 14.
At that time, the SOURCE voltage rises, which may cause detection errors in the overcurrent limiter circuit.
To prevent these detection errors, an L.E.B. function (Leading Edge Blanking function) is built in that switches the MOSFET from low to high and masks the overcurrent limiter for 250ns.
This blanking function can reduce the CS pin noise filter for noise that is generated when switching the MOSFET from low to high.

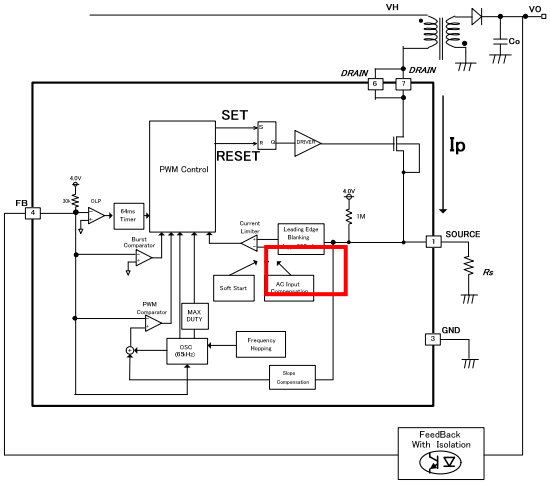
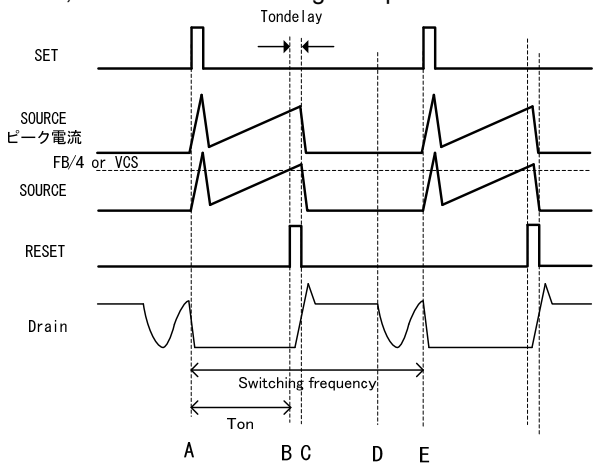


Figure 20. L.E.B. Blanking Block

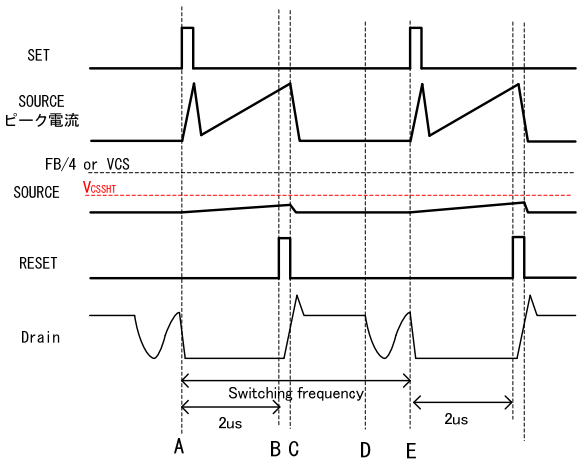
(7) SOURCE Pin Short Circuit Protection

When a short circuit occurs at the SOURCE pin, transient heat occurs in the IC, which may become damaged.
A short circuit protection circuit is built in to prevent such damage. SOURCE pin short circuit protection is turned off when the SOURCE pin voltage drops to below V_{CSSHT} (0.05V typ.) 2us after the MOSFET is turned on.
This is described in Figure 21.
When a SOURCE pin short circuit has occurred, if there is a light load the output voltage is increased and VCC OVP protection is applied.
If there is a heavy load the output voltage drops, and FBOLP protection operates.
In cases where the Lp value is low and the input voltage appears to be high, the peak current that flows after 2us has elapsed becomes larger, which may damage the MOSFET before this protection function operates.
Therefore, be careful when setting the Lp value.



1 Peak current

Figure 21-1. Normal Operation of the SOURCE Pin



1 Peak current

Figure 21-2. Short Circuit Operation of the SOURCE Pin

(8) SOURCE Pin Open Protection

When the SOURCE pin has become open, transient heat (due to noise, etc.) occurs in the IC, which may become damaged.
An open protection circuit has been built in to prevent such damage. (Auto recovery protection)

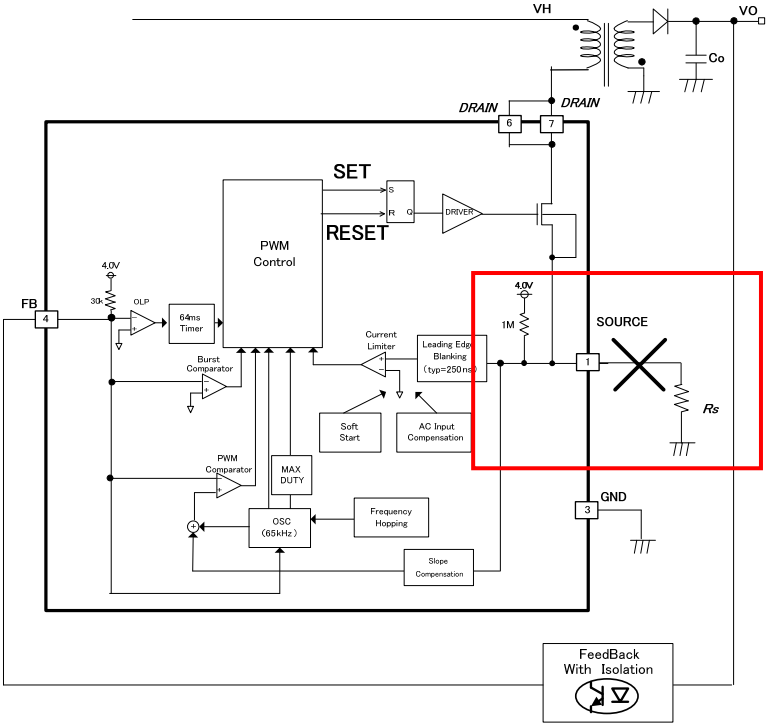


Figure 22. SOURCE Open Block

(9) Output Overload Protection Function (FB OLP Comparator)

The output overload protection function uses FB voltage to monitor the load condition of the secondary output, and stops switching when an overload condition occurs.

During an overload condition, the output voltage drops and so current no longer flows to the photocoupler and the FB voltage rises. When the FB voltage exceeds V_{FOLP1A} (2.8V typ.) continuously for T_{FOLP1} (64ms typ.), it is judged to be in overload condition and so switching is stopped. While the FB pin exceeds V_{FOLP1A} (2.8V typ.), if the FB pin voltage drops below V_{FOLP1B} (2.6V typ.) during the T_{FOLP1} (64ms typ.) period, the overload protection timer is reset. Switching operations are performed during the T_{FOLP1} (64 ms typ) period. At startup, the FB pin voltage is pulled up by a resistance to the IC internal voltage, and operations start when the voltage reaches V_{FOLP1A} (2.8V typ.) or above. Therefore, at startup the start time of the secondary output voltage must be set so that the FB voltage drops to V_{FOLP1B} (2.6V typ.) or below within the T_{FOLP1} (64ms typ.) period.

Once FBOLP is detected, recovery occurs after the T_{FOLP2} (512ms typ.) period.

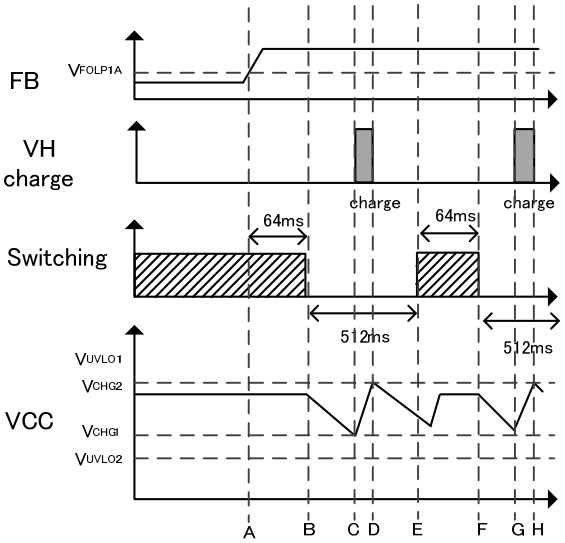


Figure 23. Overload Protection (Auto Recovery)

A: Since FB exceeds V_{FOLP1A}, the FBOLP comparator detects an overload.
B: When the condition at A continues for T_{FOLP} (64ms typ.), switching is stopped by the overload protection function.
C: While switching has been stopped by overload protection, the VCC voltage drops and when the voltage at the VCC pin becomes less than V_{CHG}, the VCC charge function operates to increase the VCC pin voltage.
D: When the VCC charge function causes the VCC pin voltage to rise above V_{CHG2}, the VCC charge function is stopped.
E: When the T_{OLPST} (512ms typ.) period that starts from time point B elapses, switching is started by soft start operation.
F: While an overload condition remains, FB continues to exceed V_{FOLP1A} and switching is stopped when the period T_{FOLP} (64 ms typ.) from time point E has elapsed.
G: While switching is stopped, the VCC voltage drops to below the VCC pin voltage V_{CHG1}, at which time the VCC charge function operates and the VCC pin voltage rises.
H: When the VCC charge function causes the VCC pin voltage to exceed V_{CHG2}, the VCC charge function is stopped.

(10-1) Notes on Board Layout Pattern [For Isolated Applications]

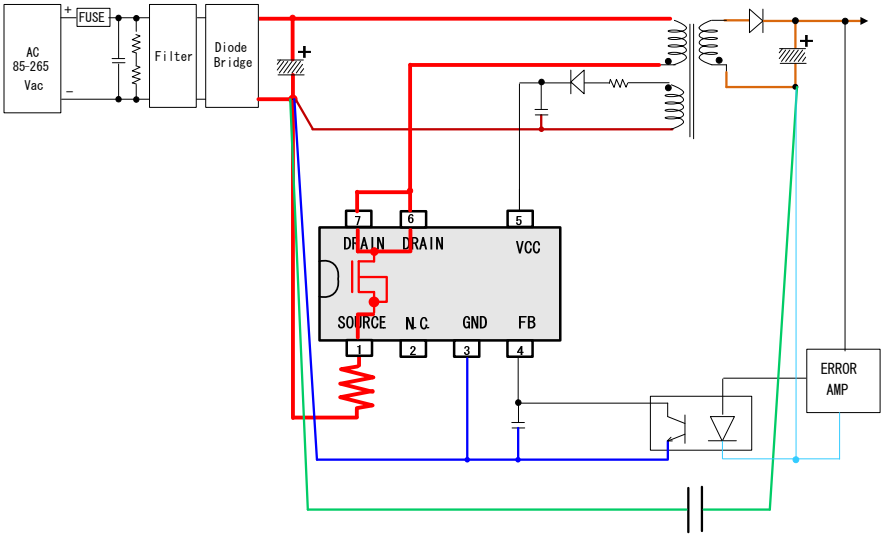


Figure 24. Board Layout Pattern

• Notes

① The red lines shown in Figure 24 are large current pathways. Therefore, in this layout, these should be as short and thick as possible since they can cause ringing, loss, etc.
Also, any loops that are generated in the red lines should be made as small as possible.

② The orange lines in the secondary side of Figure 24 should also be made short and thick like the red lines and should be made with small loops.

③ Be sure to connect the GND for the red, blue, and green lines at a single point.

④ The green lines are pathways for surges on the secondary side to escape to the primary side, and since a large current may flow instantaneously, they should be laid out independently of the red lines and blue lines.

⑤ The blue lines are GND lines for IC control. They do not have large current flow, so they are susceptible to the effects of noise. Therefore, they should be laid out independently of the red, green, and brown lines.

⑥ The brown lines are current pathways for the VCC pin. Current flows on these lines during switching, so they should also be laid out independently.

⑦ Do not route any IC control lines directly under the transformer, since they may be affected by magnetic flux.

⑧ Lay out capacitors for the VCC and FB pins as close as possible to the IC pins.

(10-2) Notes for Board Layout Pattern [For Non-Isolated Applications]

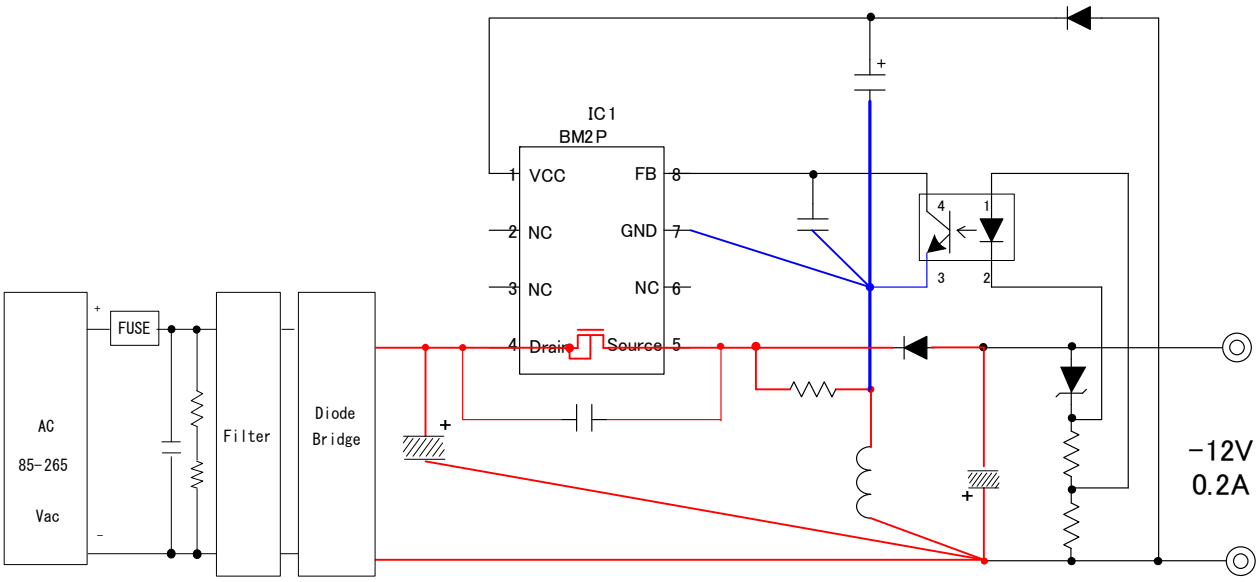


Figure 25. Board Layout Pattern

• Notes

① The red lines shown in Figure 25 are large current pathways. Therefore, in this layout, these should be as short and thick as possible since they can cause ringing, loss, etc.
Also, any loops that are generated in the red lines should be made as small as possible.

② Be sure to connect the GND of the red and blue lines at a single point.

③ The blue lines are GND lines for IC control. They do not have any large current flow, so they are susceptible to the effects of noise. Therefore, they should be laid out independently of the red lines.

④ Do not allow route high impedance lines for IC control directly under the coil due to the effects of magnetic flux.

⑤ Lay out capacitors for the VCC and FB pins as close as possible to the IC pins.

(Application Circuit Example: Isolated Application)

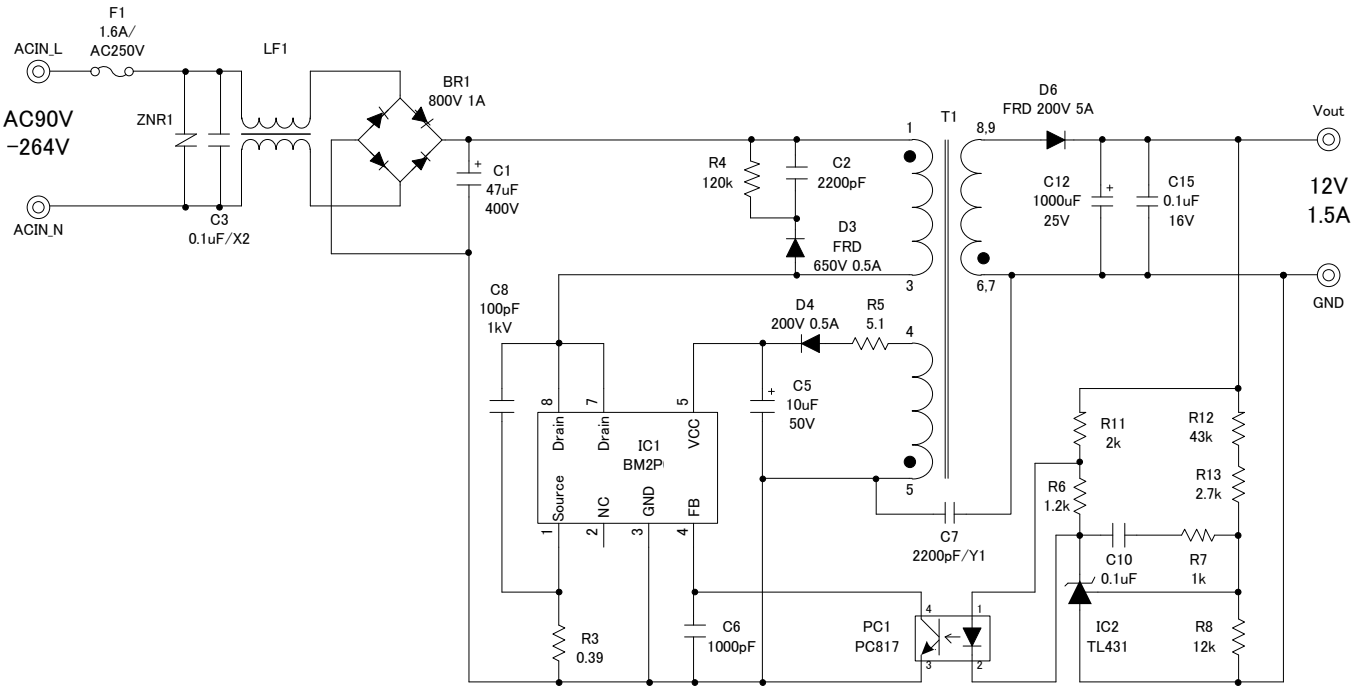


Figure 26. Application Circuit Example (Isolated)

(Application Circuit Example: Non-Isolated Application)

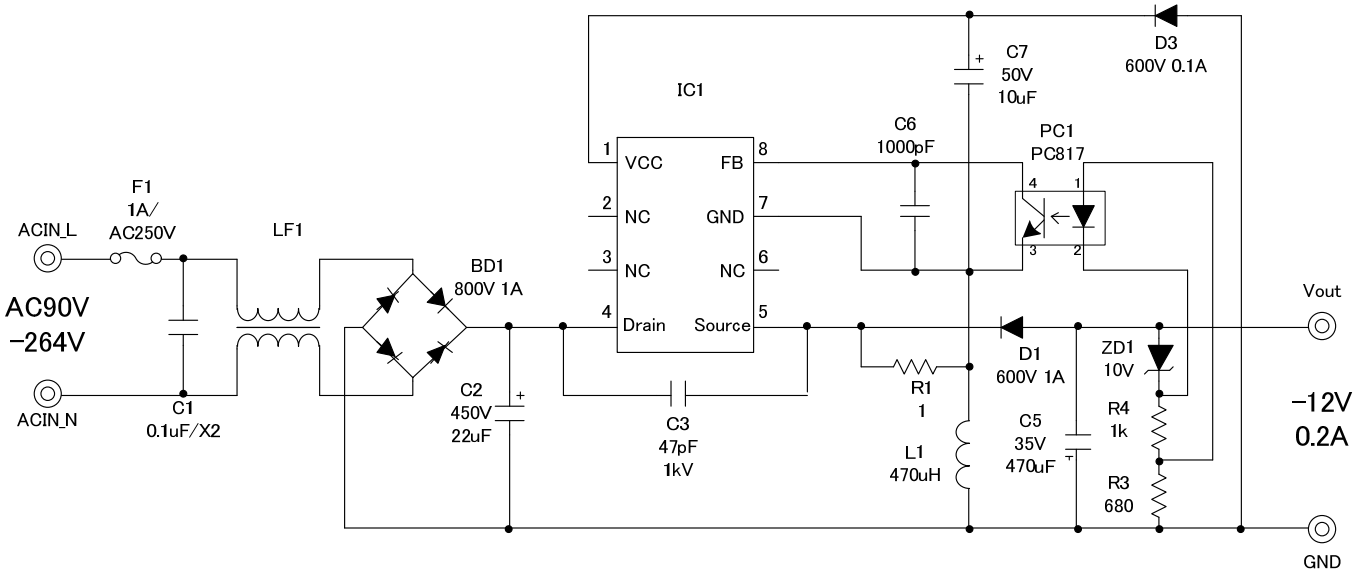


Figure 27. Application Circuit Example (Non-Isolated Negative Voltage Output)

● Operating Modes of Protection Circuit

Table 3 lists the operating mode of each protection function.

Table 3. Protection Circuit Operating Modes

Function	Operating Mode
VCC Undervoltage Lock Out	Auto-recovery
VCC Overvoltage Protection	Auto-recovery
TSD	Latch (with 100us timer)
FB Overlimit Protection	Auto-recovery (with 64ms timer)
SOURCE Short Circuit Protection	Auto-recovery
SOURCE Open Protection	Auto-recovery

● Sequence

The sequence diagram is shown in Figure 24.
A transition to OFF mode occurs under all conditions when VCC is less than 8.2V.

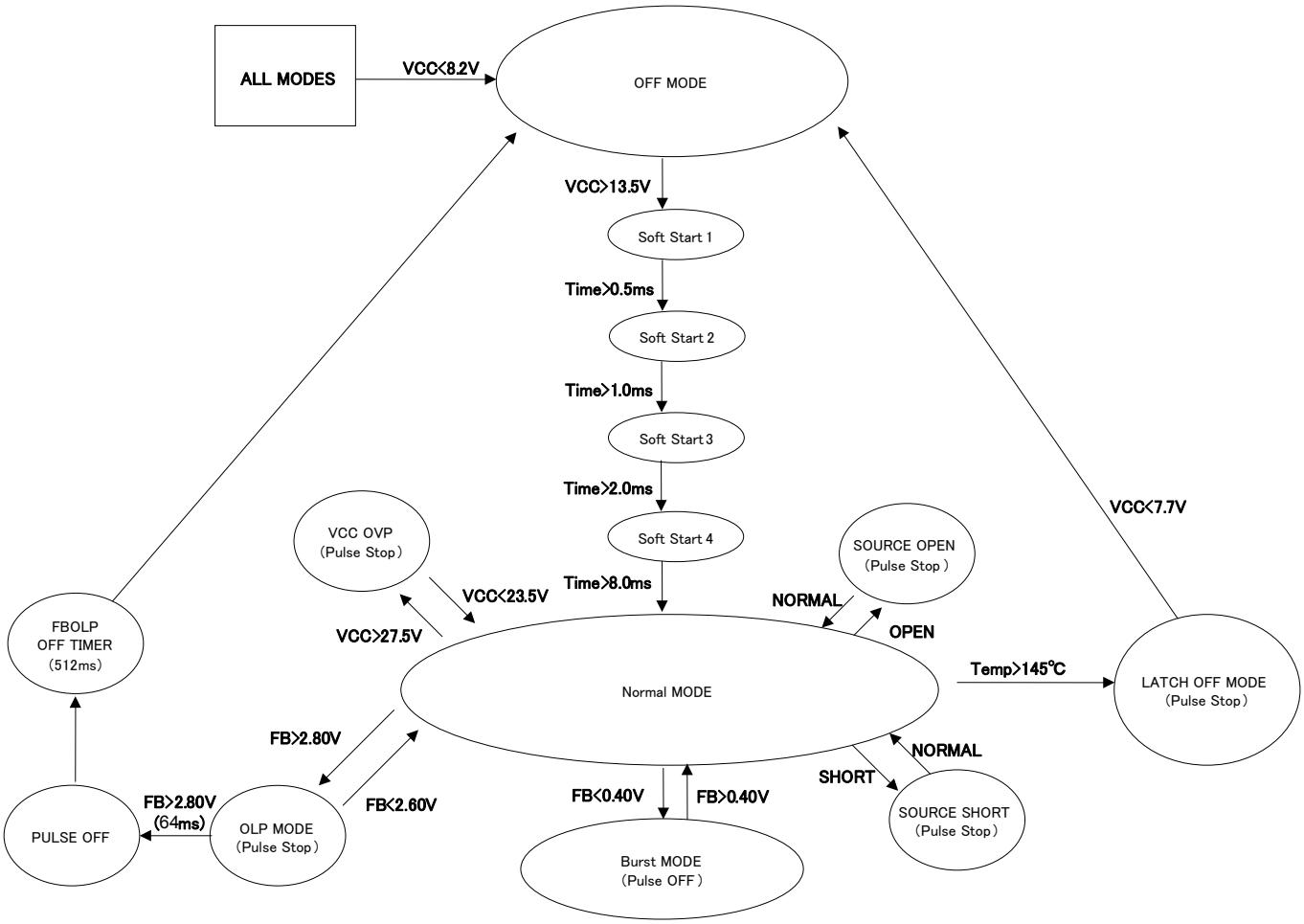


Figure 28. Sequence Diagram

● **Thermal Loss**

In the thermal design, set operations using the following conditions.

1. Ambient temperature Ta must be 105°C or less.
2. IC loss must be within the specified power dissipation Pd.

The thermal derating characteristics are as follows. (PCB: 74.2mm × 74.2mm × 1.6mm, when mounted on glass epoxy substrate)

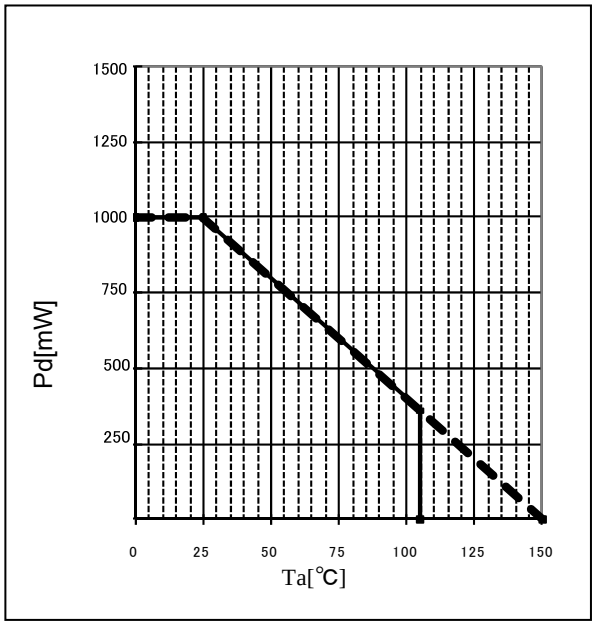


Figure 29. Thermal Derating Characteristics

● Usage Precautions

(1) Absolute maximum ratings
Damage may occur if the absolute maximum ratings are exceeded, such as for applied voltage or operating temperature range. Since the type of damage (short/open circuit, etc.) cannot be determined, in cases where a special mode may conceivably exceed the absolute maximum ratings, please consider implementing physical safety measures such as fuses.

(2) Power supply and ground lines
In the board pattern design, route the power supply and ground lines to achieve low impedance. If there are multiple power supply and ground lines, be careful about interference due to common impedance in the wiring pattern. With regard to ground lines in particular, make sure to isolate large current and small signal routes, including the external circuits. Also, for all of the power supply pins in this IC, in addition to inserting capacitors between the power supply and ground pins, please thoroughly verify any problems associated with capacitor characteristics, such as capacitance loss at low temperatures, before determining constants.

(3) Ground potential
Please set the ground pin potential to the minimum potential for all operating modes.

(4) Pin shorts and mounting errors
When mounting the IC on a board, please pay attention to the orientation and direction of the IC and possible misalignment. Incorrect mounting may damage the IC. Damage may also occur due to short circuit if foreign material is introduced between IC pins, between a pin and the power supply, or between a pin and GND.

(5) Operation in strong magnetic fields
Please note that malfunction may occur if this product is used in a strong magnetic field.

(6) Input pins
In IC structures, parasitic elements are inevitably formed in relation to the potential. The operation of parasitic elements can interfere with circuit operation, leading to malfunction and even damage. Therefore, please be careful to avoid usage methods that enable parasitic elements to operate, such as by supplying a voltage lower than the ground voltage to the input pin. Also, do not apply voltage to an input pin when there is no power supply voltage being supplied to the IC. In fact, even if power supply voltage is being supplied, the voltage supplied to each input pin should be either below the power supply voltage or within the guaranteed values in the electrical characteristics.

(7) External capacitors
When a ceramic capacitor is used as an external capacitor, please consider the possible drop in nominal capacitance due to DC bias as well as capacitance fluctuation due to temperature and the like before determining constants.

(8) Thermal design
The thermal design should take into account the power dissipation (Pd) under actual conditions. Also, please ensure that the output transistor does not exceed the rated voltage or ASO.

(9) Rush current
In a CMOS IC, rush current may momentarily flow if the internal logic is undefined when the power supply is turned ON, so caution is needed with regard to the power supply coupling capacitance, the width of power supply and GND pattern wires, and how they are laid out.

(10) Handling of test pins and unused pins
As noted in the function manual, application notes, and other documents, test pins and unused pins should be handled so as not to cause problems under actual conditions. Please contact us regarding pins that are not otherwise described.

(11) Document contents
Documents such as application notes are design resources intended for use when designing applications, and as such their contents are not guaranteed. Therefore, before finalizing an application, please conduct a thorough study and evaluation, including of the external parts.

Regarding this document
The Japanese version of this document is considered the formal specifications. Therefore, this translated version should be used only as a reference when reading the formal specifications.
Accordingly, the formal specifications take priority regarding any differences that arise in the translation.

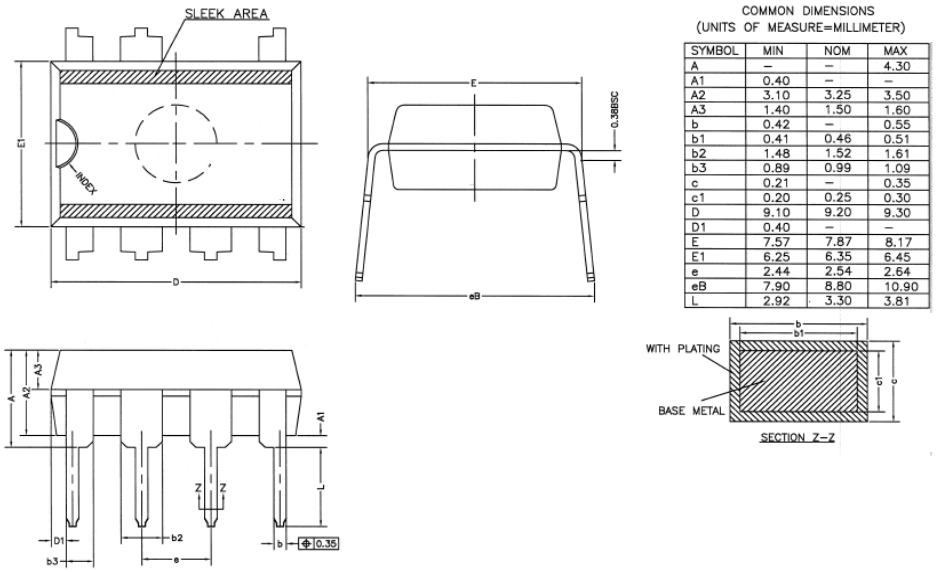
Application Notes

● **Part Number Selection**

B M 2 P X X 4	-	
Part Number	Package Blank: DIP7	Packaging and Forming Specifications Blank: Tube

●Packaging Diagram and Forming Specifications

DIP7

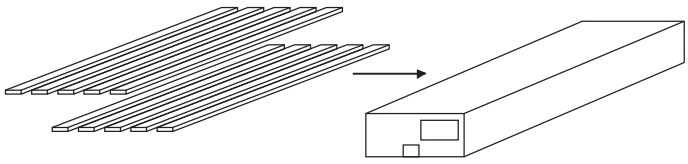


COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	4.30
A1	0.40	–	–
A2	3.10	3.25	3.50
A3	1.40	1.50	1.60
b	0.42	–	0.55
b1	0.41	0.46	0.51
b2	1.48	1.52	1.61
b3	0.89	0.99	1.09
c	0.21	–	0.35
c1	0.20	0.25	0.30
D	9.10	9.20	9.30
D1	0.40	–	–
E	7.57	7.87	8.17
E1	6.25	6.35	6.45
e	2.44	2.54	2.64
eB	7.90	8.80	10.90
L	2.92	3.30	3.81

<Tape and Reel information>

Container	Tube
Quantity	2000pcs
Direction of feed	Direction of products is fixed in a container tube

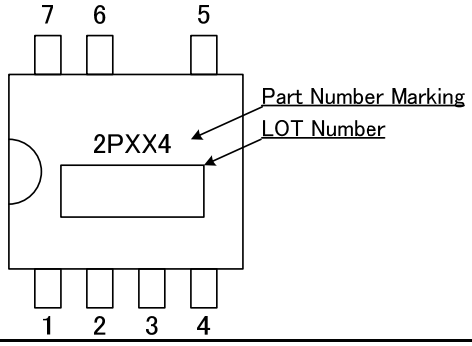


∗Order quantity needs to be multiple of the minimum quantity.

1 <Packaging Specifications> 2 Packaging Type Container Tube 3 Package quantity
4 Feed direction 5 Products are in same direction in each container tube
6 * Order in multiples of the package count.

● Marking Code

DIP7



● Lineup

Part No. (BM2PXX4)
BM2P014
BM2P034
BM2P054
BM2P094

Notes

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2) Before you use our Products, please contact our sales representative and verify the latest specifications :

3) Although ROHM is continuously working to improve product reliability and quality, semiconductors can break down and malfunction due to various factors.
Therefore, in order to prevent personal injury or fire arising from failure, please take safety measures such as complying with the derating characteristics, implementing redundant and fire prevention designs, and utilizing backups and fail-safe procedures. ROHM shall have no responsibility for any damages arising out of the use of our Poducts beyond the rating specified by ROHM.

4) Examples of application circuits, circuit constants and any other information contained herein are provided only to illustrate the standard usage and operations of the Products. The peripheral conditions must be taken into account when designing circuits for mass production.

5) The technical information specified herein is intended only to show the typical functions of and examples of application circuits for the Products. ROHM does not grant you, explicitly or implicitly, any license to use or exercise intellectual property or other rights held by ROHM or any other parties. ROHM shall have no responsibility whatsoever for any dispute arising out of the use of such technical information.

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7) The Products specified in this document are not designed to be radiation tolerant.

8) For use of our Products in applications requiring a high degree of reliability (as exemplified below), please contact and consult with a ROHM representative : transportation equipment (i.e. cars, ships, trains), primary communication equipment, traffic lights, fire/crime prevention, safety equipment, medical systems, servers, solar cells, and power transmission systems.

9) Do not use our Products in applications requiring extremely high reliability, such as aerospace equipment, nuclear power control systems, and submarine repeaters.

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ROHM SEMICONDUCTOR

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