FEDL-7660-01
Issue Date: Oct. 5, 2021

ML7660

13.56MHz wireless charging Rx LSI

1. Overview

ML7660 is a 13.56MHz wireless power receiving device. ML7660 realizes a wireless power receiving system by combining with the power transmission device ML7661, and can output 1W for power receiving.
The ML7660 is equipped with a 10-bit SA-ADC for measuring the power supply status and a wireless power supply control function in a 2.28 mm x 2.61 mm (equivalent to 2.44 mm square) WL-CSP chip or a 5 mm square 32-pin WQFN package. This LSI is ideal for wireless power supply of small devices. In addition, since it is equipped with the NFC Forum Type 3 Tag function, it is possible to realize NFC functions such as Bluetooth® pairing by touch. Furthermore, ML7660 is equipped with a host interface (SPI / I²C slave) function and a serial interface (SPI / I²C master, UART) function, and it is possible to update configuration data from an external MCU and control various sensors.

2. Features

- Charging control
  - Built-in Charging control circuit
    Built-in setting of output voltage by shunt regulator
    Voltage/Current supply ON/OFF function to external charging IC
    1W receiving available
  - Abnormaly detection by software and hardware control
  - Abnormaly notifivation function to the power transmission side

- NFC communication control
  - NFC Forum Type3 TAG function uncluded
  - Communication speed: 212kbps, 424kbps
  - 2Kbyte data flash for storing TAG data contents

- Host interface
  - 1ch Serial interface (Slave), and selectable from SPI or I²C
  - Register function accessible from the host MCU
  - Built-in 512byte FIFO

- Serial interface
  - 1ch SPI interface(Master)
  - 1ch I²C interface(Master)
  - 1ch UART interface (2-wire, Full-duplex communication mode)

- General Port(PORT)
  - Input/Output port×13ch

- Successive approximation type A/D converter (SA-ADC)
  - Resolution 10bit

- Reset
  - Reset by RESET_N port
  - Power on reset
  - Reset by WDT overflow

ROHM SEMICONDUCTOR

- Clock
  - Low speed clock
    Built-in RC oscillation(32.768kHz)
  - High speed clock
    RX0/RX1 antenna input(13.56MHz) from magnetic field

- Package
  - WL-CSP30pin (S-UFLGA30-2.28x2.61-0.40-W)
  - WQFN32pin (P-WQFN32-0505-0.50-A63)

- CPU
  - 16-bit RISC CPU（CPU：nX-U16/100）
  - Built-in On-chip debug function
  - Minimum instruction execution time
    - ✧ 18.86us（@212kHz system clock）

- Internal memory
  - Memory size

Flash*	SRAM	Other RAM
Program：32K byte Data：2K byte	6K byte（Work RAM） 1K byte(For debugger trace function)	256 byte（For NFC） 512 byte (For Host interface)

*: This product uses SuperFlash® technology licensed from Silicon Storage Technology, Inc.
SuperFlash® is a registered trademark of Silicon Storage Technology, Inc.

- Interrupt controller (INTC)
  - 1 non-maskable interrupt source (Internal source: WDT)
  - 26 maskable interrupt sources(Internal source: 18, External source: 8）
  - Software interrupt(SWI): Max. 64 sources
  - Selectable edge and sampling for external interrupt and comparator
  - Four step unterrupt levels

- Timer
  - 8bit×8ch (16-bit configuration is possible using 2ch)
  - Built-in Repeat mode, One shot mode is available
  - Timer start/stop function by software

- Watchdog timer(WDT)
  - Non-maskable interrupt and Reset
    1st overflow: generate interrupt, 2nd overflow: generate reset or host notification
  - Free-run
  - Overflow period: 4 selectable(125ms, 500ms, 2s, 8s) at LSCLK=32.768kHz
  - Stop function

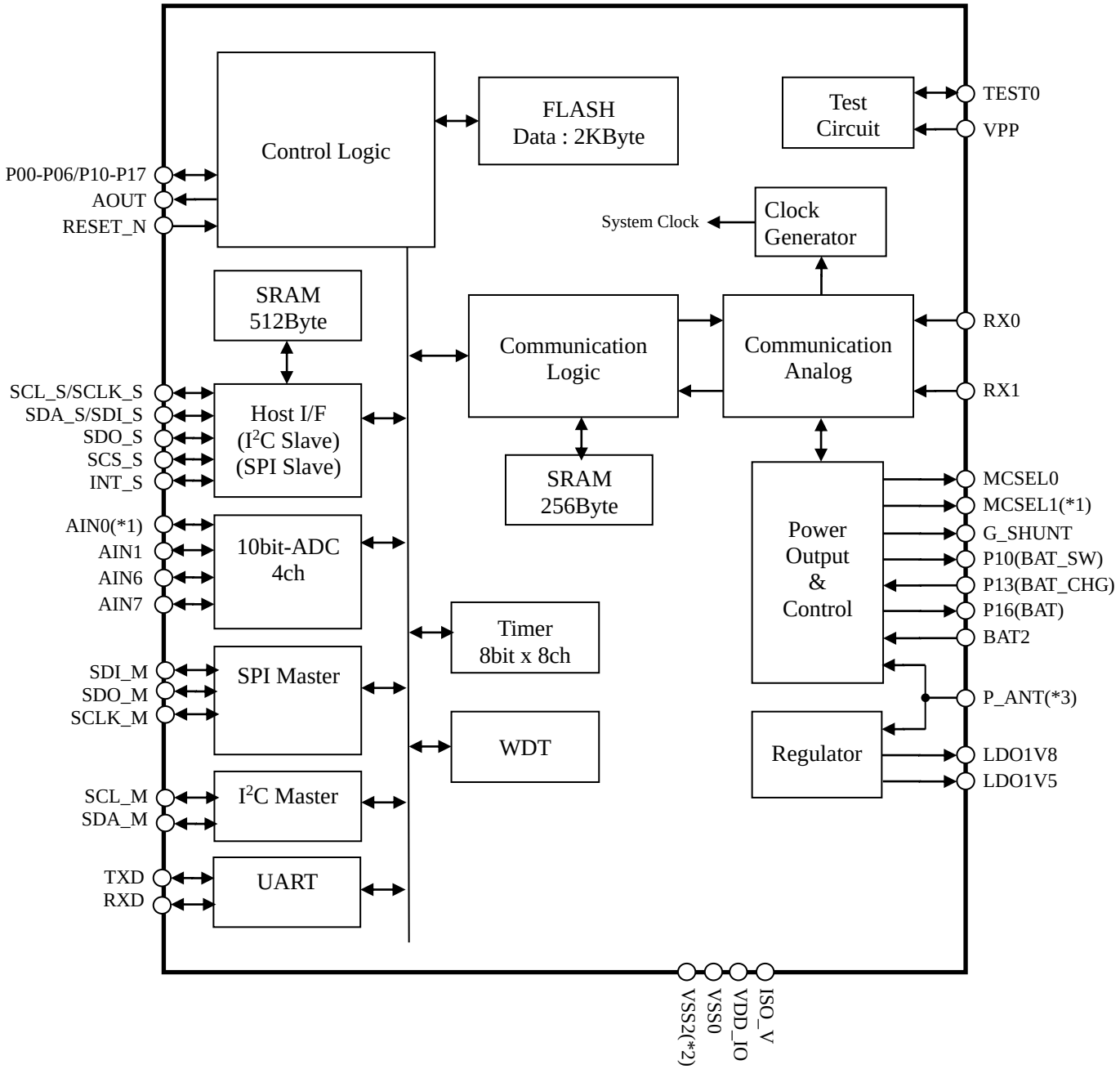
- I^2C bus interface (I^2C Master)
  - Normal mode (100kbit/s), Fast mode (400kbit/s) available

- SPI interface (SPI Master)
  - Selectable from MSB/LSB first
  - Selectable from 8-bit length or 16-bit length
  - Selectable clock phase and polarity

- UART
  - Full-duplex communication mode
  - Communication speed: 4800 to 115200bps
  - Programable interface (Data length, Parity and Stop bit can be selected)

- Power management
  - Clock division function
    System clock supports 6.78MHz, 3.39MHz, 1.7MHz, 848kHz, 424kHz, 212kHz and 106kHz
  - Clock stop function
    HALT mode to stop only CPU

3. Functional block structure



*1 WQFN32pin only
*2 WL-CSP30pin only
*3 In WL-CSP 30pin, P_ANT is connected to VDD_IO inside the LSI

4. Pin assignment

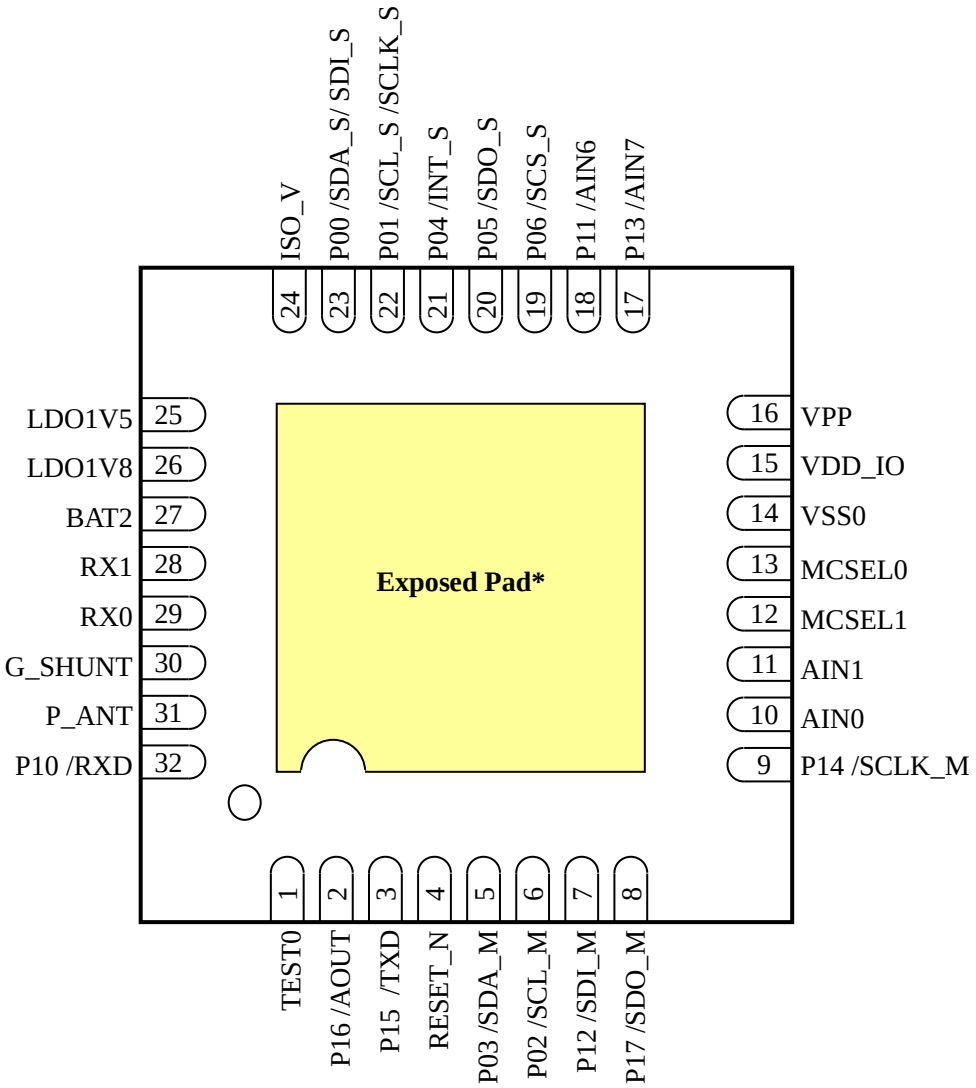
WL-CSP 30pin

BOTTOM VIEW

P13 / AIN7	VDD_IO	MCSEL0	AIN1	P14 / SCLK_M	6
P06 / SCS_S	P11 / AIN6	VPP	P17 / SDO_M	P12 / SDI_M	5
P04 / INT_S	P05 / SDO_S	VSS0	P02 / SCL_M	P03 / SDA_M	4
P00 / SDA_S / SDI_S	P01 / SCL_S / SCLK_S	VSS2	P15 / TXD	P16 / AOUT	3
ISO_V	RESET_N	TEST0	RX1	P10 / RXD	2
LDO1V5	LDO1V8	BAT2	RX0	G_SHUNT	1
E	D	C	B	A	

WQFN 32pin

TOP VIEW



*Solder the exposed pad onto the PCB

5. Pin description

5.1 Power GND reference voltage pins

PIN No.	Pin name	In reset (*1)	I/O (*2)	Active Level	Description	Process in not use
C4/14	VSS0	—	—	—	Ground (VSS0 to VSS2 are connected inside the LSI, respectively)	—
C3	VSS2					
D6/15	VDD_IO	—	—	—	Logic IO voltage	—
E1/25	LDO1V5	H(A)	O_A	—	Core 1.5V voltage output	—
D1/26	LDO1V8	H(A)	O_A	—	ADC 1.8V voltage output	—
31	P_ANT	—	—	—	Rectify input (In CSP, this pin is connected to VDD_IO by WL-CSP wiring)	—
E2/24	ISO_V	—	—	—	Logic IO voltage (for host communication)	—
C1/27	BAT2	—	I_A	—	Battery voltage monitoring	—

5.2 Analog signal pins

PIN No.	Pin name	In reset (*1)	I/O (*2)	Active Level	Description	Process in not use
B1/29	RX0	—	I_A	—	Antenna（Plus） / Data receiving	—
B2/28	RX1	—	I_A	—	Antenna（Minus） / Data receiving	—

5.3 Other Pins

PIN No.	Pin name	In reset (*1)	I/O (*2)	Supply power	Active Level	Description	Process in not use
D2/4	RESET_N	PU	I	VDD_IO	L	Reset input /For debugger	Open
E3/23	P00 / SDA_S / SDI_S	Z	I/O	ISO_V	—	Input/Output port HostIF(I^2C slave) Data input/Output HostIF(SPI slave) Data input	Open
D3/22	P01 / SCL_S / SCLK_S	Z	I/O	ISO_V	—	Input/Output port HostIF(I^2C slave) Clock input HostIF(SPI slave) Clock input	Open
B4/6	P02 / SCL_M	Z	I/O	ISO_V	—	Input/Output port I^2C master clock output	Open
A4/5	P03 / SDA_M	Z	I/O	ISO_V	—	Input/Output port I^2C master data input/output	Open
E4/21	P04 / INT_S	Z	I/O	ISO_V	—	Input/Output port HostIF INT output	Open
D4/20	P05 / SDO_S	Z	I/O	ISO_V	—	Input/Output port HostIF(SPI slave) data output	Open
E5/19	P06 / SCS_S	Z	I/O	ISO_V	—	Input/Output port HostIF(SPI slave) select signal	Open
10	AIN0	Z	I_A	VDD_IO	—	AD input 0	Open
B6/11	AIN1	Z	I_A	VDD_IO	—	AD input 1 for current measurement	Open
A2/32	P10(BAT_SW) / RXD	PU	I/O	VDD_IO	—	Input/Output port(Power supply ON/OFF) UART data input	Open
D5/18	P11 / AIN6	Z	I_{DA}/O	ISO_V	—	Input/Output port/AD input 6	Open

PIN No.	Pin name	In reset (*1)	I/O (*2)	Supply power	Active Level	Description	Process in not use
A5/7	P12 / SDI_M	Z	I/O	ISO_V	–	Input/Output port SPI master data input	Open
E6/17	P13 (BAT_CHG) / AIN7	Z	I_{DA}/O	VDD_IO	–	Input/Output port (interrupt input for Charging IC) AD input 7	Open
A6/9	P14 / SCLK_M	Z	I/O	ISO_V	–	Input/Output port SPI master clock output	Open
B3/3	P15 / TXD	Z	I/O	VDD_IO	–	Input/Output port UART data output	Open
A3/2	P16(BAT) / AOUT	Z	I/O_{DA}	VDD_IO	–	Input/Output port (Discharge of input charge for Charging IC) Analog monitor output	Open
B5/8	P17 / SDO_M	Z	I/O	ISO_V	–	Input/Output port SPI master data output	Open
C6/13	MCSEL0	PU	O	VDD_IO	–	Matching capacitor select signal	Open
12	MCSEL1	PU	O	VDD_IO	–	Matching capacitor select signal	Open
A1/30	G_SHUNT	L(A)	O	P_ANT	–	Shunt transistor control signal	Open

5.4 Test pins

PIN No.	Pin name	In reset (*1)	I/O (*2)	Supply power	Active Level	Description	Process in not use
C2/1	TEST0	Z	I/O	VDD_IO	L	For test/For debugger	Pull-Up
C5/16	VPP	–	I_A	–	–	Power supply for Flash test	Open

(*1) In reset state :

Pin state definition in reset state	L(O)	:	“L” level output
	H(O)	:	“H” level output
	L(A)	:	Analog “L” level output
	H(A)	:	Analog “H” level output
	PU	:	Pull-Up
	PD	:	Pull-Down
	Z	:	Floating state

(*2) I/O : For I/O definition, using under abbreviation

I/O definition	I_A	:	Analog input
	O_A	:	Analog output
	I	:	Digital input
	I/O	:	Bi-directional pin
	I_{DA}/O	:	Bi-directional pin, Input are digital and analog shared
	I/O_{DA}	:	Bi-directional pin, Output are digital and analog shared
	O	:	Digital output

6. Electrical characteristics

6.1 Absolute maximum ratings

Item	Symbol	Condition	Rating	Unit
Power voltage	VDD_IO	Ta=25°C	-0.3 to +6.5	V
	ISO_V	Ta=25°C	-0.3 to +6.5	V
	P_ANT	Ta=25°C	-0.3 to +6.5	V
	BAT2	Ta=25°C	-0.3 to +6.5	V
Core power voltage	LDO1V5	Ta=25°C	-0.3 to +2.0	V
Analog power voltage	LDO1V8	Ta=25°C	-0.3 to +6.5	V
Input voltage	V_{DIN}	Ta=25°C, Digital port	-0.3 to V_{DD}+0.3	V
		Ta=25°C, RX0/RX1	12	V
Input current	Ii	Ta=25°C, Digital port	-10 to +10	mA
	I_{P_ANT}	Ta=25°C	100	mA
Output voltage	V_{DO}	Ta=25°C, Digital port	-0.3 to V_{DD}+0.3	V
Digital output current	I_{DO}	Ta=25°C	-12 to +20	mA
Power dissipation (QFN)	PD	Ta=25°C	1	W
Power dissipation (CSP)	PD	Ta=25°C	0.5	W
Storage temperature	Tstg	—	-55 to +150	°C

V_{DD} : Refer to Pin Description table, in case “Supply Power” column equals “VDD_IO”, VDD is VDD_IO voltage and column equals “ISO_V”, VDD is ISO_V voltage.

6.2 Recommended operating conditions

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating voltage	VDD_IO	—	1.8	—	5.5	V
	ISO_V	—	1.8	—	5.5	V
	P_ANT	Communication	2.0	5.0	5.5	V
		Charging	—	—	5.5	V
Operating temperature	Ta	Communication	-40	+25	+85	°C
LDO1V5 outside Capacitor	C_{LDO1V5}	—	Typ -10%	2.2	Typ +10%	µF
P_ANT outside Capacitor	C_{PANT}	—	Typ -10%	2.2	Typ +10%	µF
LDO1V8 outside Capacitor	C_{LDO1V8}	—	Typ -10%	0.47	Typ +10%	µF
VDD_IO outside Capacitor	C_{VDDIO}	—	Typ -10%	0.1	Typ +10%	µF
ISO_V outside Capacitor	C_{ISOV}	—	Typ -10%	0.1	Typ +10%	µF
Antenna input frequency	F_{ANT}	—	Typ -0.05%	13.56	Typ +0.05%	MHz
AIN input voltage	V_{AIN}	AIN0,AIN6,AIN7	0	—	1.8	V

6.3 Flash memory operating conditions

Item	Symbol	Condition	Range	Unit
Operating temperature (Ambience)	T_{OP}	write/erase	-20 to +60	°C
Operating voltage	P_ANT	write/erase	2.7 to 5.5	V
Rewrite count	C_{EPD}	Program Flash	100	Times
		Data Flash	10,000	Times
Erase unit	–	Sector erase (Program Flash)	1	KB
		Sector erase (Data Flash)	128	B
Erase time (Maximum)	–	Sector erase	50	ms
Write unit	–	Program Flash	4 bytes	–
		Data Flash	1 byte	–

6.4 RF characteristics

(VDD_IO=1.8 to 5.5V, P_ANT=2.0 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Level	V_{RX1}	RX0/RX1	2.0	–	5.9	V
Input data amplitude	V_{RX2}	RX0/RX1	50	–	–	mV
Communication speed	F_{RX}	RX0/RX1		212		kbps
				424		kbps

6.5 Notification characteristics

(VDD_IO=1.8 to 5.5V, P_ANT=2.0 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
P_ANT limiter	V_{PANT1}	Normal	–	–	5.5	V
	V_{PANT2}	In case of abnormality notice	–	3.0	–	V

6.6 Oscillation characteristics

(VDD_IO=1.8 to 5.5V, P_ANT=2.0 to 5.5V, VSS=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Low speed embedded RC oscillator frequency *1	f_{LCR}		-10%	32.768	+10%	kHz

*1 : 1024 cycle average

6.7 SA-ADC characteristics

(VDD_IO=1.8 to 5.5V, P_ANT=2.0 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n	—	–	10	–	bit
Integral non-linearity error	INL	LDO1V8=1.8V	-6	–	+6	LSB
Differential non-linearity error	DNL	LDO1V8=1.8V	-6	–	+6	LSB
Zero scale error	ZSE	—	-6	–	+6	LSB
Full scale error	FSE	—	-6	–	+6	LSB
Input impedance	RI	—	–	6k	–	Ω
SA-ADC reference voltage	V_{REF}	LDO1V8=V_{REF}	–	1.8	–	V

6.8 Reset characteristics

(VDD_IO=1.8 to 5.5V, P_ANT=2.0 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
RESET_N pulse width	P_{RST}	—	2	–	–	ms
RESET_N noise removal Pulse width	P_{NRST}	—	–	–	0.3	µs

6.9 AC characteristics (I^2C Bus Interface)

● Standard Mode 100kHz

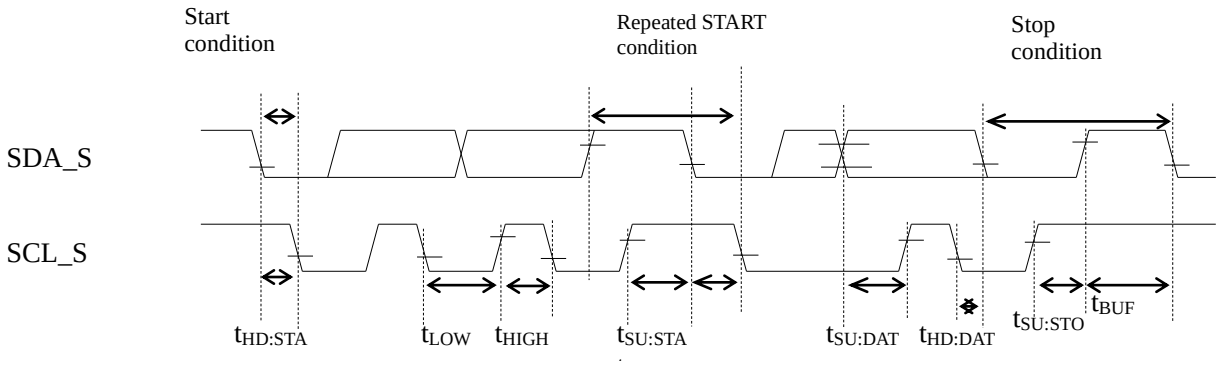
(VDD_IO/ISO_V=1.8 to 5.5V, P_ANT=2.0 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL_S clock frequency	f_{SCL}	–	–	–	100	kHz
SCL_S hold time (start/repeated start condition)	$t_{HD:STA}$	–	4.0	–	–	µs
SCL_S "L" level time	t_{LOW}	–	4.7	–	–	µs
SCL_S "H" level time	t_{HIGH}	–	4.0	–	–	µs
SCL_S setup time (repeated start condition)	$t_{SU:STA}$	–	4.7	–	–	µs
SDA_S hold time	$t_{HD:DAT}$	–	0	–	–	µs
SDA_S setup time	$t_{SU:DAT}$	–	0.25	–	–	µs
SDA_S setup time (P: Stop condition)	$t_{SU:STO}$	–	4.0	–	–	µs
Bus free time	t_{BUF}	–	4.7	–	–	µs

● Fast Mode 400kHz

(VDD_IO/ISO_V=1.8 to 5.5V, P_ANT=2.0 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL_S clock frequency	f_{SCL}	–	–	–	400	kHz
SCL_S hold time (start/repeated start condition)	$t_{HD:STA}$	–	0.6	–	–	µs
SCL_S "L" level time	t_{LOW}	–	1.3	–	–	µs
SCL_S "H" level time	t_{HIGH}	–	0.6	–	–	µs
SCL_S setup time (repeated start condition)	$t_{SU:STA}$	–	0.6	–	–	µs
SDA_S hold time	$t_{HD:DAT}$	–	0	–	–	µs
SDA_S setup time	$t_{SU:DAT}$	–	0.1	–	–	µs
SDA_S setup time (P: Stop condition)	$t_{SU:STO}$	–	0.6	–	–	µs
Bus free time	t_{BUF}	–	1.3	–	–	µs

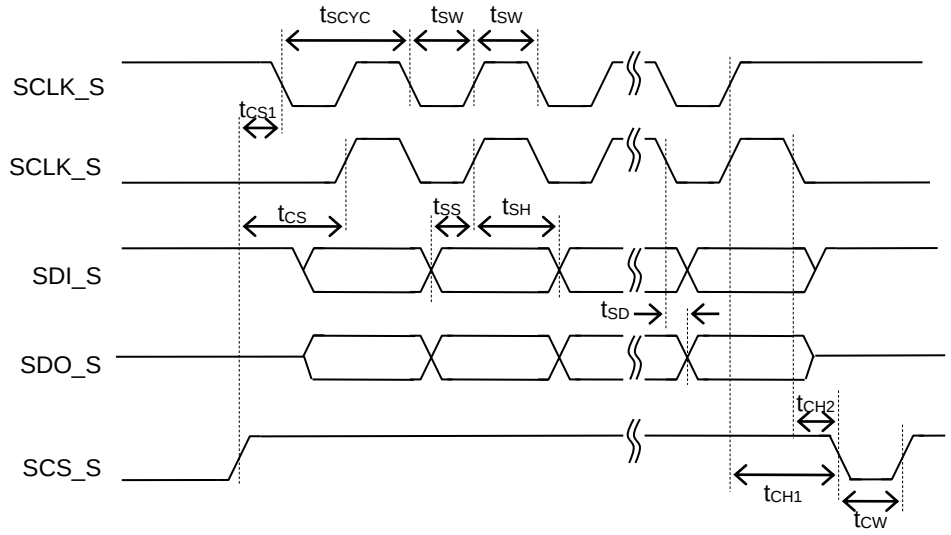


If powering off ISO_V of this LSI, it disables communications of other devices on the I^2C bus.
If there is a power supply of ISO_V of this LSI even if powering off P_ANT of this LSI, SDA_S/SCL_S maintains Hi-z state.

6.10 AC characteristics (Host Interface: SPI slave)

(VDD_IO/ISO_V=1.8 to 5.5V, P_ANT=2.0 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
SCLK_S input cycle	t_{SCYC}	–	500	–	–	ns
SCLK_S input pulse width	t_{SW}	–	200	–	–	ns
SCS_S setup time	t_{CS1}	–	80	–	–	ns
	t_{CS2}	–	80	–	–	ns
SCS_S hold time	t_{CH1}	–	80	–	–	ns
	t_{CH2}	–	80	–	–	ns
SCS_S input pulse width	t_{CW}	–	80	–	–	ns
SDO_S output delay time	t_{SD}	–	–	–	240	ns
SDI_S input setup time	t_{SS}	–	80	–	–	ns
SDI_S input hold time	t_{SH}	–	80	–	–	ns

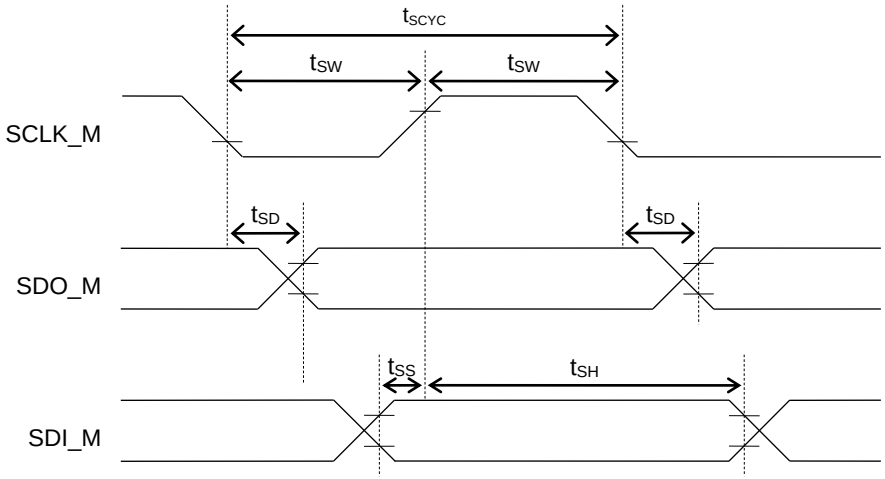


6.11 AC characteristics (SPI master)

(VDD_IO/ISO_V=1.8 to 5.5V, P_ANT=2.0 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
SCLK_M output cycle	t_{SCYC}	–	–	SCLK*1	–	s
SCLK_M output pulse width	t_{SW}	–	t_{SCYC} ×0.4	t_{SCYC} ×0.5	t_{SCYC} ×0.6	s
SDO_M output delay time	t_{SD}	–	–	–	100	ns
SDI_M input setup time	t_{SS}	–	100	–	–	ns
SDI_M input hold time	t_{SH}	–	60	–	–	ns

*1 : The Period of the internal clock selected by the interface register



6.12 IO characteristics

(Unless otherwise specified,VDD_IO=1.8 to 5.5V, P_ANT=2.0 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Output voltage 1 (P00-P07, P10-P17)	VOH1	IOH=-1.0mA	V_{DD}-0.5	–	–	V
	VOL1	IOL=+0.5mA	–	–	0.4	V
Output voltage 2 (P00-P07, P10-P17) (LED mode selected)	VOL2	2.7V ≤ V_{DD} ≤ 5.5V IOL=+5.0mA	–	–	0.6	V
		IOL=+2.0mA	–	–	0.4	V
Output voltage 3 (P00-P03) (I^2C mode selected)	VOL3	IOL3= +3mA (I^2C spec) (VDD_IO ≥ 2V、ISO_V ≥ 2V)	–	–	0.4	V
Output voltage 4 (P00-P03) (I^2C mode selected)	VOL4	IOL4= +2mA (I^2C spec) (VDD_IO < 2V、ISO_V < 2V)	–	–	V_{DD}×0.2	V
Output leakage 1 (P00-P07, P10-P17)	IOOH1	VOH=V_{DD} (at high impedance)	–	–	1	μA
	IOOL1	VOL=VSS (at high impedance)	-1	–	–	μA
Input current 1 (RESET_N, TEST1_N)	IIH1	VIH1=V_{DD}	–	–	1	μA
	IIL1	VIL1=VSS	-900	-300	-20	μA
Input current 2 (TEST0)	IIH2	VIH2=V_{DD}	–	–	1	μA
	IIL2	VIL2=VSS	-200	-15	-1	μA
Input current 3 (P00-P07, P10-P17)	IIH3	VIH3=V_{DD} (In pull down)	1	15	200	μA
	IIL3	VIL3=VSS (In pull down)	-200	-15	-1	μA
	IIH3Z	VIH3=V_{DD} (at high impedance)	–	–	1	μA
	IIL3Z	VIL3=VSS (at high impedance)	-1	–	–	μA
Input voltage 1 (RESET_N, TEST0, P00-P07, P10-P17)	VIH1	–	0.75×V_{DD}	–	V_{DD}	V
	VIL1	–	0	–	0.3×V_{DD}	V
Input pin capacitance (RESET_N, TEST0, P00-P07, P10-P17)	CIN	f=10kHz Vrms=50mV Ta=25°C	–	10	–	pF
Leak current	I_{ISOV}	Voltage supply to the ISO_V terminal,no magnetic field input	–	100	–	nA

V_{DD} : Refer to Pin Description table, in case "Supply Power" column equals "VDD_IO", VDD is VDD_IO voltage and column equals "ISO_V", VDD is ISO_V voltage.
Typ. standard is at Ta=25°C, VDD_IO=3.0V

6.13 Current consumption

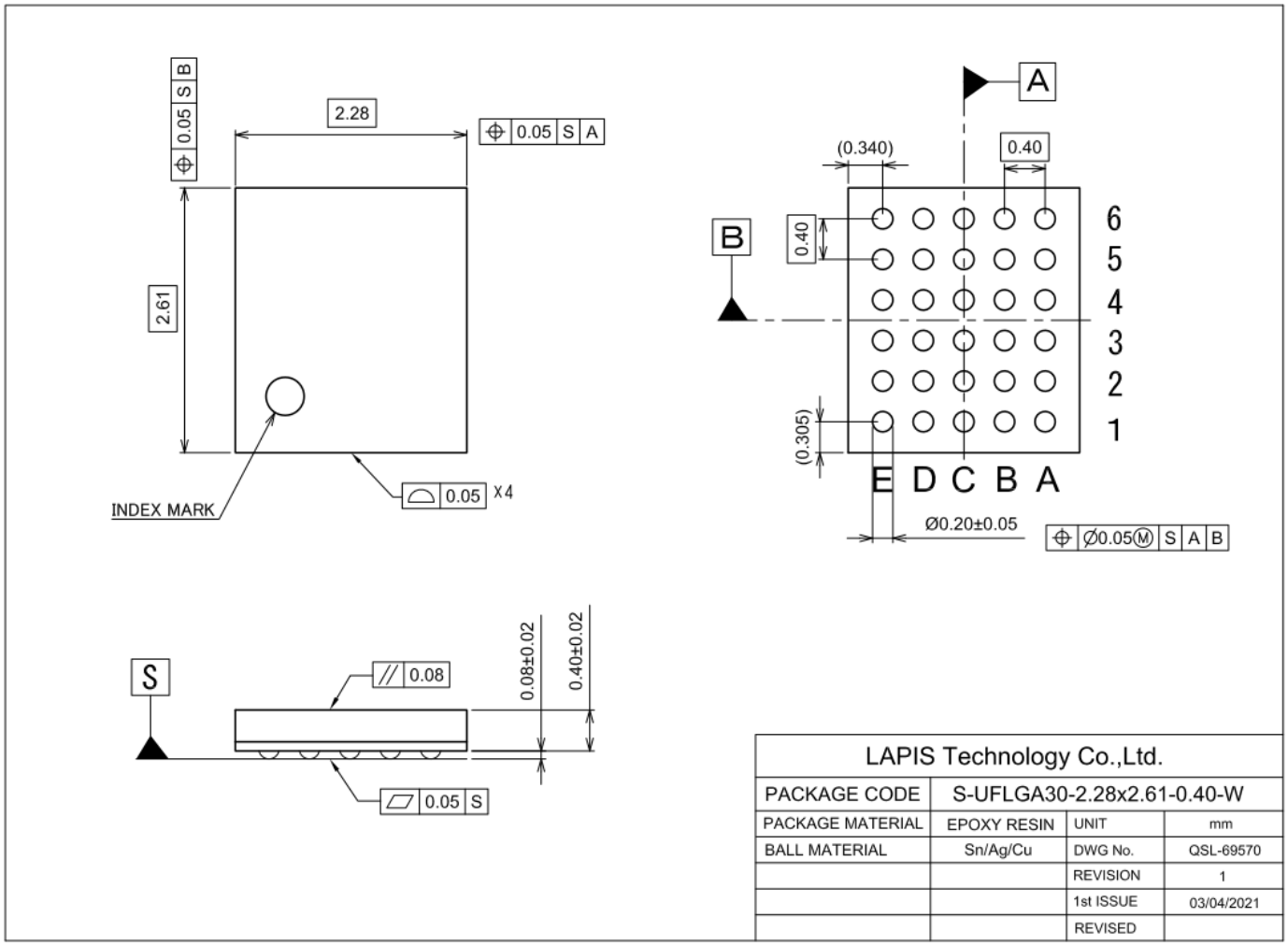
(VDD_IO=1.8 to 5.5V, P_ANT=4.5 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Current consumption	P_ANT	Communication	0.5	–	–	mA
		Charging	–	–	10	mA

* Current consumption depends on the antenna design. The smaller the load resistance, the higher the current consumption. External Transistor is not included.

7. Package dimensions

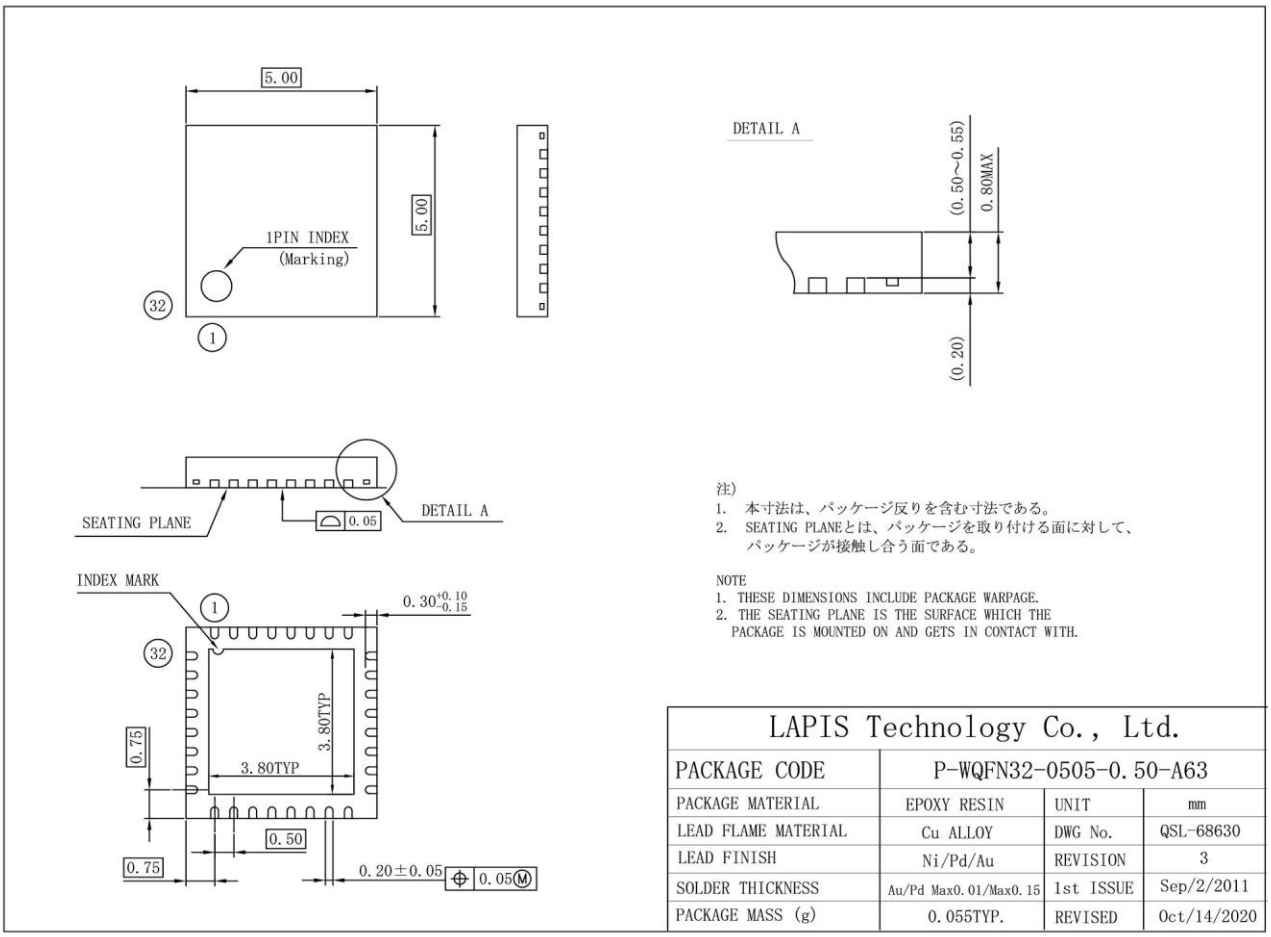
WL-CSP30pin



LAPIS Technology Co.,Ltd.			
PACKAGE CODE	S-UFLGA30-2.28x2.61-0.40-W		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
BALL MATERIAL	Sn/Ag/Cu	DWG No.	QSL-69570
		REVISION	1
		1st ISSUE	03/04/2021
		REVISED	

Notes for Mounting the Surface Mount Type Package
The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

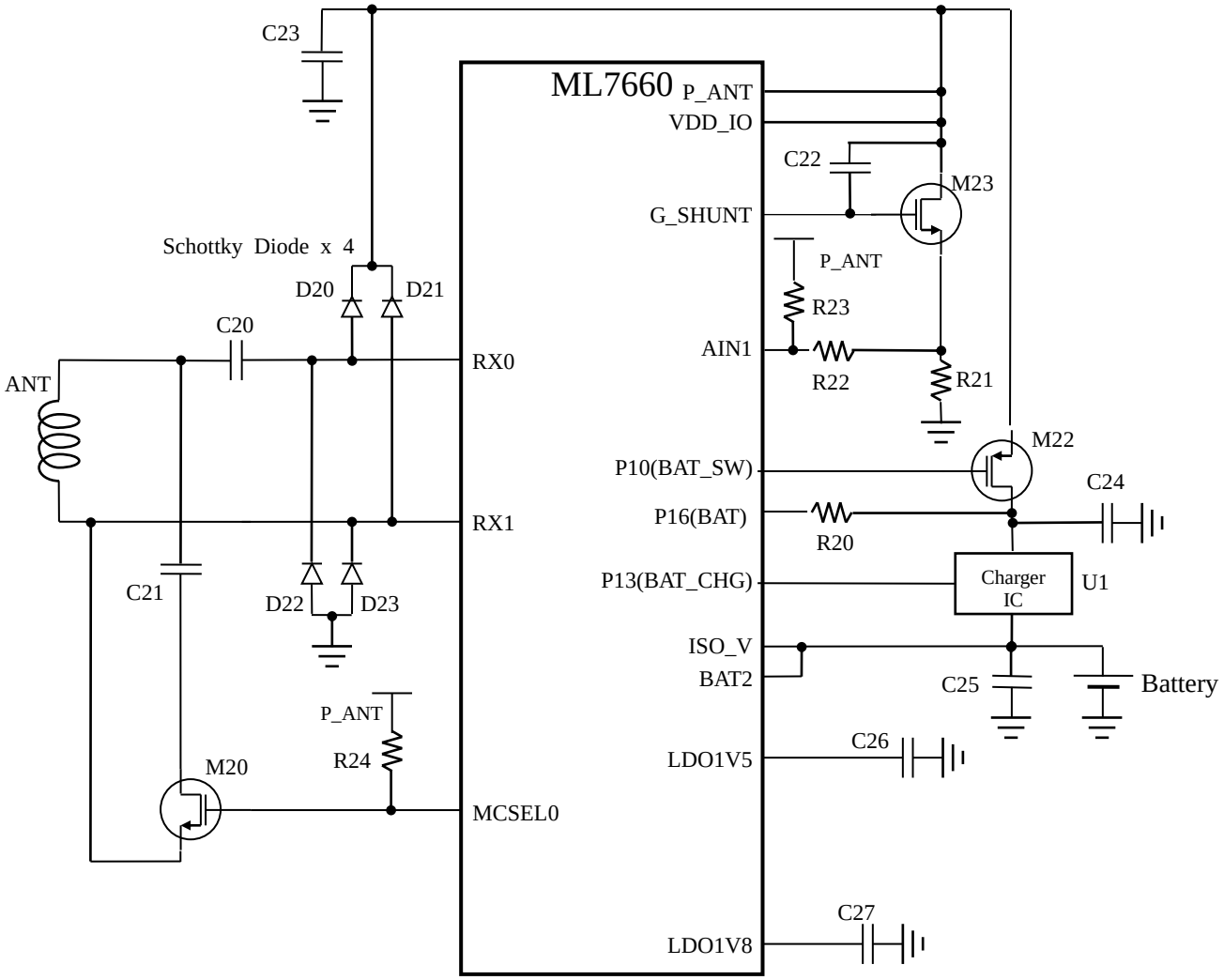
WQFN32pin



LAPIS Technology Co., Ltd.			
PACKAGE CODE	P-WQFN32-0505-0.50-A63		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-68630
LEAD FINISH	Ni/Pd/Au	REVISION	3
SOLDER THICKNESS	Au/Pd Max0.01/Max0.15	1st ISSUE	Sep/2/2011
PACKAGE MASS (g)	0.055TYP.	REVISED	Oct/14/2020

Notes for Mounting the Surface Mount Type Package
The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

8. Sample circuit



Mandatory Parts List

Parts Name	Parts Number	Value	Size	Manufacturer	Description
Capacitor	C20	150pF, over 100V	1005	Murata	GRM155 Series
	C21	100pF, over 100V	1005	Murata	GRM155 Series
	C22	470pF	1005	Murata	GRM155 Series
	C27	0.47µF	1005	Murata	GRM155 Series
	C23, C26	2.2µF	1005	Murata	GRM155 Series
	C24, C25	1µF, Decoupling Capacitor	1005	Murata	GRM155 Series
Resistor	R20	10kΩ, For discharge	1005	ROHM	MCR01 Series
	R21	1Ω	1005	ROHM	MCR01 Series
	R22	330Ω	1005	ROHM	MCR01 Series
	R23	10kΩ	1005	ROHM	MCR01 Series
	R24	100kΩ	1005	ROHM	MCR01 Series
MOS Transistor	M20	NMOS, 60V, 0.25A	2924	ROHM	RK7002BM
	M22	PMOS, 20V, 1.5A	2020	ROHM	QS6M4(Dual)
	M23	NMOS, 20V, 1.5A	2020	ROHM	QS6M4(Dual)
Schottky Diode	D20, D21, D22, D23	Ifmax=5A,Vf=360mV, Vr=20V	2508	ROHM	RB162VAM-20
Charger IC	U1	-			
Battery		-			
ANT		-			

Revision history

Document No.	Issue Date	Page		Change contents
		Previous Edition	Current Edition	
FEDL7660-01	2021.10.5	–	–	First edition

Notes

1) The information contained herein is subject to change without notice.

2) When using LAPIS Technology Products, refer to the latest product information (data sheets, user's manuals, application notes, etc.), and ensure that usage conditions (absolute maximum ratings, recommended operating conditions, etc.) are within the ranges specified. LAPIS Technology disclaims any and all liability for any malfunctions, failure or accident arising out of or in connection with the use of LAPIS Technology Products outside of such usage conditions specified ranges, or without observing precautions. Even if it is used within such usage conditions specified ranges, semiconductors can break down and malfunction due to various factors. Therefore, in order to prevent personal injury, fire or the other damage from break down or malfunction of LAPIS Technology Products, please take safety at your own risk measures such as complying with the derating characteristics, implementing redundant and fire prevention designs, and utilizing backups and fail-safe procedures. You are responsible for evaluating the safety of the final products or systems manufactured by you.

3) Descriptions of circuits, software and other related information in this document are provided only to illustrate the standard operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. And the peripheral conditions must be taken into account when designing circuits for mass production. LAPIS Technology disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, and other related information.

4) No license, expressly or implied, is granted hereby under any intellectual property rights or other rights of LAPIS Technology or any third party with respect to LAPIS Technology Products or the information contained in this document (including but not limited to, the Product data, drawings, charts, programs, algorithms, and application examples、etc.). Therefore LAPIS Technology shall have no responsibility whatsoever for any dispute, concerning such rights owned by third parties, arising out of the use of such technical information.

5) The Products are intended for use in general electronic equipment (AV/OA devices, communication, consumer systems, gaming/entertainment sets, etc.) as well as the applications indicated in this document. For use of our Products in applications requiring a high degree of reliability (as exemplified below), please be sure to contact a LAPIS Technology representative and must obtain written agreement: transportation equipment (cars, ships, trains, etc.), primary communication equipment, traffic lights, fire/crime prevention, safety equipment, medical systems, servers, solar cells, and power transmission systems, etc. LAPIS Technology disclaims any and all liability for any losses and damages incurred by you or third parties arising by using the Product for purposes not intended by us. Do not use our Products in applications requiring extremely high reliability, such as aerospace equipment, nuclear power control systems, and submarine repeaters, etc.

6) The Products specified in this document are not designed to be radiation tolerant.

7) LAPIS Technology has used reasonable care to ensure the accuracy of the information contained in this document. However, LAPIS Technology does not warrant that such information is error-free and LAPIS Technology shall have no responsibility for any damages arising from any inaccuracy or misprint of such information.

8) Please use the Products in accordance with any applicable environmental laws and regulations, such as the RoHS Directive. LAPIS Technology shall have no responsibility for any damages or losses resulting non-compliance with any applicable laws or regulations.

9) When providing our Products and technologies contained in this document to other countries, you must abide by the procedures and provisions stipulated in all applicable export laws and regulations, including without limitation the US Export Administration Regulations and the Foreign Exchange and Foreign Trade Act..

10) Please contact a ROHM sales office if you have any questions regarding the information contained in this document or LAPIS Technology's Products.

11) This document, in part or in whole, may not be reprinted or reproduced without prior consent of LAPIS Technology.

(Note) "LAPIS Technology" as used in this document means LAPIS Technology Co., Ltd.

LAPIS Technology Co.,Ltd.
2-4-8 Shinyokohama, Kouhoku-ku, Yokohama 222-8575, Japan
https://www.lapis-tech.com/en/